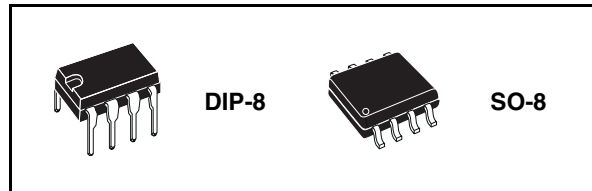


## High-voltage half bridge driver

### Features

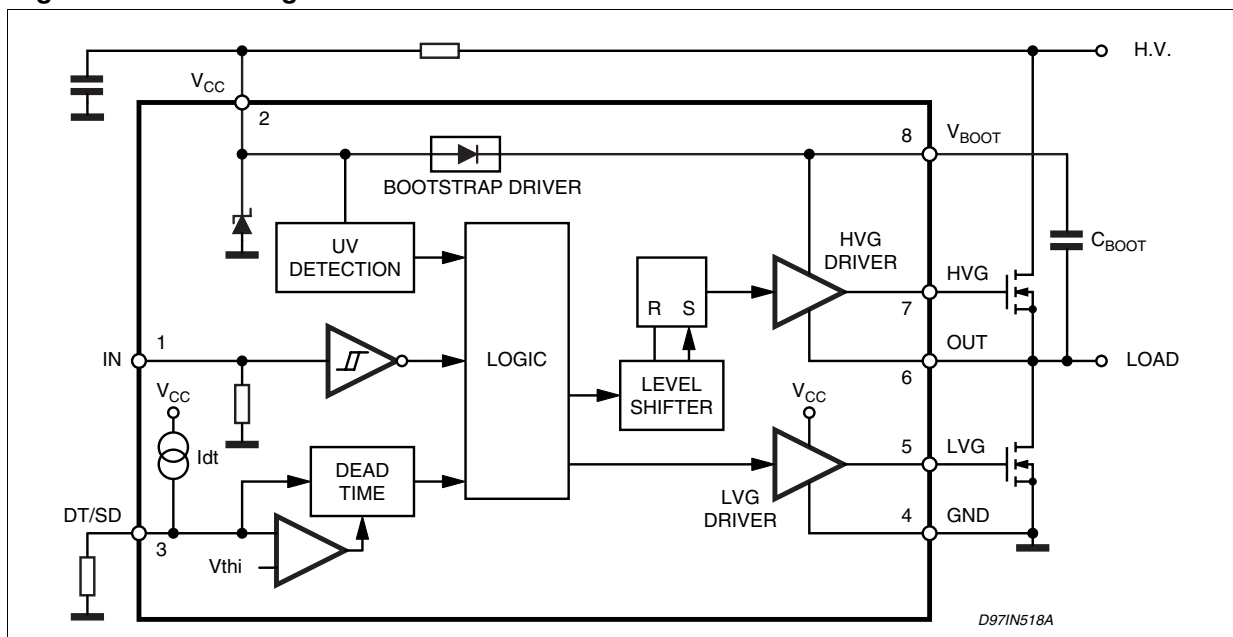
- High voltage rail up to 600V
- $dV/dt$  immunity  $\pm 50V/nsec$  in full temperature range
- Driver current capability:
  - 400mA source,
  - 650mA sink
- Switching times 50/30 nsec rise/fall with 1nF load
- CMOS/TTL Schmitt trigger inputs with hysteresis and pull down
- Shut down input
- Dead time setting
- Under voltage lock out
- Integrated bootstrap diode
- Clamping on  $V_{CC}$
- SO-8/DIP-8 packages



### Description

The L6384E is an high-voltage device, manufactured with the BCD"OFF-LINE" technology. It has an Half - Bridge Driver structure that enables to drive N-channel Power MOS or IGBT. The High Side (Floating) Section is enabled to work with voltage Rail up to 600V. The Logic Inputs are CMOS/TTL compatible for ease of interfacing with controlling devices. Matched delays between Low and High Side Section simplify high frequency operation. Dead time setting can be readily accomplished by means of an external resistor.

**Figure 1. Block diagram**



# Contents

<b>1</b>	<b>Electrical data</b> .....	<b>3</b>
1.1	Absolute maximum ratings .....	3
1.2	Thermal data .....	3
1.3	Recommended operating conditions .....	4
<b>2</b>	<b>Pin connection</b> .....	<b>5</b>
<b>3</b>	<b>Electrical characteristics</b> .....	<b>6</b>
3.1	AC operation .....	6
3.2	DC operation .....	6
3.3	Timing diagram .....	7
<b>4</b>	<b>Bootstrap driver</b> .....	<b>8</b>
4.1	C <sub>BOOT</sub> selection and charging .....	8
<b>5</b>	<b>Typical characteristic</b> .....	<b>10</b>
<b>6</b>	<b>Package mechanical data</b> .....	<b>12</b>
<b>7</b>	<b>Order codes</b> .....	<b>15</b>
<b>8</b>	<b>Revision history</b> .....	<b>16</b>

# 1 Electrical data

## 1.1 Absolute maximum ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{out}$	Output voltage	-3 to $V_{boot} - 18$	V
$V_{cc}$	Supply voltage <sup>(1)</sup>	- 0.3 to 14.6	V
$I_s$	Supply current <sup>(1)</sup>	25	mA
$V_{boot}$	Floating supply voltage	-1 to 618	V
$V_{hvg}$	High side gate output voltage	-1 to $V_{boot}$	V
$V_{lvg}$	Low side gate output voltage	-0.3 to $V_{cc} + 0.3$	V
$V_i$	Logic input voltage	-0.3 to $V_{cc} + 0.3$	V
$V_{sd}$	Shut down/dead time voltage	-0.3 to $V_{cc} + 0.3$	V
$dV_{out}/dt$	Allowed output slew rate	50	V/ns
$P_{tot}$	Total power dissipation ( $T_j = 85\text{ °C}$ )	750	mW
$T_j$	Junction temperature	150	°C
$T_s$	Storage temperature	-50 to 150	°C

1. The device has an internal Clamping Zener between GND and the  $V_{cc}$  pin, It must not be supplied by a Low Impedence Voltage Source.

*Note:* ESD immunity for pins 6, 7 and 8 is guaranteed up to 900 V (Human Body Model)

## 1.2 Thermal data

**Table 2. Thermal data**

Symbol	Parameter	SO-8	DIP-8	Unit
$R_{th(JA)}$	Thermal Resistance Junction to ambient	150	100	°C/W

### 1.3 Recommended operating conditions

**Table 3. Recommended operating conditions**

Symbol	Pin	Parameter	Test condition	Min	Typ	Max	Unit
$V_{out}$	6	Output Voltage		(1)		580	V
$V_{BS}^{(2)}$	8	Floating Supply Voltage		(1)		17	V
$f_{sw}$		Switching Frequency	HVG,LVG load $C_L = 1nF$			400	kHz
$V_{cc}$	2	Supply Voltage				$V_{clamp}$	V
$T_j$		Junction Temperature		-45		125	°C

1. If the condition  $V_{boot} - V_{out} < 18V$  is guaranteed,  $V_{out}$  can range from -3 to 580V.

2.  $V_{BS} = V_{boot} - V_{out}$

## 2 Pin connection

Figure 2. Pin connection (Top view)

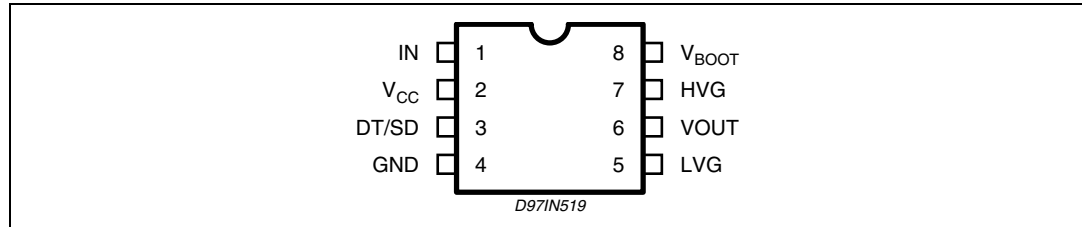


Table 4. Pin description

N°	Pin	Type	Function
1	IN	I	Logic Input: it is in phase with HVG and in opposition of phase with LVG. It is compatible to $V_{CC}$ voltage. [ $V_{il\ Max} = 1.5V$ , $V_{ih\ Min} = 3.6V$ ]
2	$V_{CC}$		Supply input voltage: there is an internal clamp [Typ. 15.6V]
3	DT/SD	I	High impedance pin with two functionalities. When pulled lower than $V_{dt}$ [Typ. 0.5V] the device is shut down. A voltage higher than $V_{dt}$ sets the dead time between high side gate driver and low side gate driver. The dead time value can be set forcing a certain voltage level on the pin or connecting a resistor between pin 3 and ground. Care must be taken to avoid below threshold spikes on pin 3 that can cause undesired shut down of the IC. For this reason the connection of the components between pin 3 and ground has to be as short as possible. This pin can not be left floating for the same reason. The pin has not be pulled through a low impedance to $V_{CC}$ , because of the drop on the current source that feeds $R_{dt}$ . The operative range is: $V_{dt} \dots 270K \cdot I_{dt}$ , that allows a dt range of 0.4 - 3.1 $\mu s$ .
4	GND		Ground
5	LVG	O	Low Side Driver Output: the output stage can deliver 400mA source and 650mA sink [Typ. Values]. The circuit guarantees 0.3V max on the pin (@ $I_{sink} = 10mA$ ) with $V_{CC} > 3V$ and lower than the turn on threshold. This allows to omit the bleeder resistor connected between the gate and the source of the external mosfet normally used to hold the pin low; the gate driver ensures low impedance also in SD conditions.
6	$V_{out}$	O	High Side Driver Floating Reference: layout care has to be taken to avoid below ground spikes on this pin.
7	HVG	O	High Side Driver Output: the output stage can deliver 400mA source and 650mA sink [Typ. Values]. The circuit guarantees 0.3V max between this pin and $V_{out}$ (@ $I_{sink} = 10mA$ ) with $V_{CC} > 3V$ and lower than the turn on threshold. This allows to omit the bleeder resistor connected between the gate and the source of the external mosfet normally used to hold the pin low; the gate driver ensures low impedance also in SD conditions.
8	Vboot		Bootstrap Supply Voltage: it is the high side driver floating supply. The bootstrap capacitor connected between this pin and pin 6 can be fed by an internal structure named "bootstrap driver" (a patented structure). This structure can replace the external bootstrap diode.

### 3 Electrical characteristics

#### 3.1 AC operation

**Table 5. AC operation electrical characteristics** ( $V_{CC} = 14.4V$ ;  $T_J = 25^\circ C$ )

Symbol	Pin	Parameter	Test condition	Min	Typ	Max	Unit
$t_{on}$	1 vs 5,7	High/low side driver turn-on propagation delay	$V_{out} = 0V$ $R_{dt} = 47k\Omega$		200+ dt		ns
$t_{onsd}$	3 vs 5,7	Shut down input propagation delay			220	280	ns
$t_{off}$	1 vs 5,7	High/low side driver turn-off propagation delay	$V_{out} = 0V$ $R_{dt} = 47k\Omega$		250	300	ns
			$V_{out} = 0V$ $R_{dt} = 146k\Omega$		200	250	ns
			$V_{out} = 0V$ $R_{dt} = 270k\Omega$		170	200	ns
$t_r$	5,7	Rise time	$C_L = 1000pF$		50		ns
$t_f$	5,7	Fall time	$C_L = 1000pF$		30		ns

#### 3.2 DC operation

**Table 6. DC operation electrical characteristics** ( $V_{CC} = 14.4V$ ;  $T_J = 25^\circ C$ )

Symbol	Pin	Parameter	Test condition	Min	Typ	Max	Unit
<b>Supply voltage section</b>							
$V_{clamp}$	2	Supply voltage clamping	$I_s = 5mA$	14.6	15.6	16.6	V
$V_{ccth1}$	2	$V_{CC}$ UV turn on threshold		11.5	12	12.5	V
$V_{ccth2}$	2	$V_{CC}$ UV turn off threshold		9.5	10	10.5	V
$V_{cchys}$		$V_{CC}$ UV Hysteresis			2		V
$I_{qccu}$		Undervoltage quiescent supply current	$V_{cc} \leq 11V$		150		$\mu A$
$I_{qcc}$		Quiescent current	$V_{in} = 0$		380	500	$\mu A$
<b>Bootstrapped supply voltage section</b>							
$V_{boot}$	8	Bootstrap supply voltage				17	V
$I_{QBS}$		Quiescent current	$IN = HIGH$			200	$\mu A$
$I_{LK}$		High voltage leakage current	$V_{hvg} = V_{out} = V_{boot} = 600V$			10	$\mu A$
$R_{dson}$		Bootstrap driver on resistance <sup>(1)</sup>	$V_{cc} \geq 12.5V$ ; $IN = LOW$		125		$\Omega$

**Table 6. DC operation electrical characteristics** (continued)( $V_{CC} = 14.4V$ ;  $T_J = 25^\circ C$ )

Symbol	Pin	Parameter	Test condition	Min	Typ	Max	Unit
<b>High/Low side driver</b>							
$I_{SO}$	5,7	Source short circuit current	$V_{IN} = V_{ih}$ ( $t_p < 10\mu s$ )	300	400		mA
$I_{SI}$		Sink short circuit current	$V_{IN} = V_{il}$ ( $t_p < 10\mu s$ )	500	650		mA
<b>Logic inputs</b>							
$V_{il}$	1,3	Low level logic threshold voltage				1.5	V
$V_{ih}$		High level logic threshold voltage		3.6			V
$I_{ih}$		High level logic input current	$V_{IN} = 15V$		50	70	$\mu A$
$I_{il}$		Low level logic input current	$V_{IN} = 0V$			1	$\mu A$
$I_{ref}$	3	Dead time setting current			28		$\mu A$
dt	3 vs 5,7	Dead time setting range <sup>(2)</sup>	$R_{dt} = 47k\Omega$ $R_{dt} = 146k\Omega$ $R_{dt} = 270k\Omega$	0.4	0.5 1.5 2.7	3.1	$\mu s$ $\mu s$ $\mu s$
$V_{dt}$	3	Shutdown threshold			0.5		V

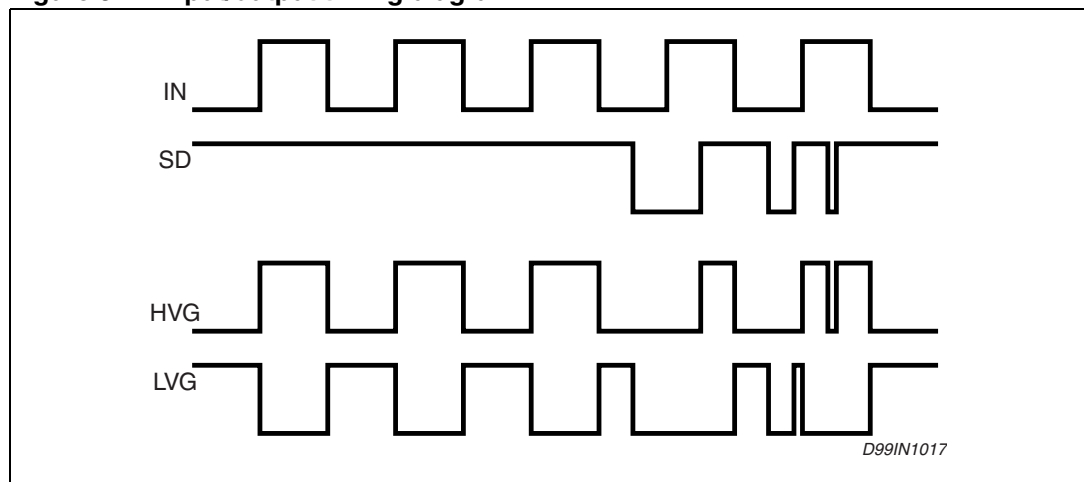
1.  $R_{DS(on)}$  is tested in the following way:

$$R_{DS(on)} = \frac{(V_{CC} - V_{CBOOT1}) - (V_{CC} - V_{CBOOT2})}{I_1(V_{CC}, V_{CBOOT1}) - I_2(V_{CC}, V_{CBOOT2})}$$

where  $I_1$  is pin 8 current when  $V_{CBOOT} = V_{CBOOT1}$ ,  $I_2$  when  $V_{CBOOT} = V_{CBOOT2}$

2. Pin 3 is a high impedance pin. Therefore dt can be set also forcing a certain voltage  $V_3$  on this pin. The dead time is the same obtained with a  $R_{dt}$  if it is:  $R_{dt} \times I_{ref} = V_3$ .

### 3.3 Timing diagram

**Figure 3. Input/output timing diagram**

## 4 Bootstrap driver

A bootstrap circuitry is needed to supply the high voltage section. This function is normally accomplished by a high voltage fast recovery diode (*Figure 4 a*). In the L6384E a patented integrated structure replaces the external diode. It is realized by a high voltage DMOS, driven synchronously with the low side driver (LVG), with in series a diode, as shown in *Figure 4 b*. An internal charge pump (*Figure 4 b*) provides the DMOS driving voltage. The diode connected in series to the DMOS has been added to avoid undesirable turn on of it.

### 4.1 C<sub>BOOT</sub> selection and charging

To choose the proper C<sub>BOOT</sub> value the external MOS can be seen as an equivalent capacitor. This capacitor C<sub>EXT</sub> is related to the MOS total gate charge:

$$C_{EXT} = \frac{Q_{gate}}{V_{gate}}$$

The ratio between the capacitors C<sub>EXT</sub> and C<sub>BOOT</sub> is proportional to the cyclical voltage loss. It has to be:

$$C_{BOOT} \gg C_{EXT}$$

e.g.: if Q<sub>gate</sub> is 30nC and V<sub>gate</sub> is 10V, C<sub>EXT</sub> is 3nF. With C<sub>BOOT</sub> = 100nF the drop would be 300mV.

If HVG has to be supplied for a long time, the C<sub>BOOT</sub> selection has to take into account also the leakage losses.

e.g.: HVG steady state consumption is lower than 200µA, so if HVG T<sub>ON</sub> is 5ms, C<sub>BOOT</sub> has to supply 1µC to C<sub>EXT</sub>. This charge on a 1µF capacitor means a voltage drop of 1V.

The internal bootstrap driver gives great advantages: the external fast recovery diode can be avoided (it usually has great leakage current).

This structure can work only if V<sub>OUT</sub> is close to GND (or lower) and in the meanwhile the LVG is on. The charging time (T<sub>charge</sub>) of the C<sub>BOOT</sub> is the time in which both conditions are fulfilled and it has to be long enough to charge the capacitor.

The bootstrap driver introduces a voltage drop due to the DMOS R<sub>DSON</sub> (typical value: 125 Ω). At low frequency this drop can be neglected. Anyway increasing the frequency it must be taken in to account.

The following equation is useful to compute the drop on the bootstrap DMOS:

$$V_{drop} = I_{charge} R_{dson} \rightarrow V_{drop} = \frac{Q_{gate}}{T_{charge}} R_{dson}$$

where Q<sub>gate</sub> is the gate charge of the external power MOS, R<sub>dson</sub> is the on resistance of the bootstrap DMOS, and T<sub>charge</sub> is the charging time of the bootstrap capacitor.

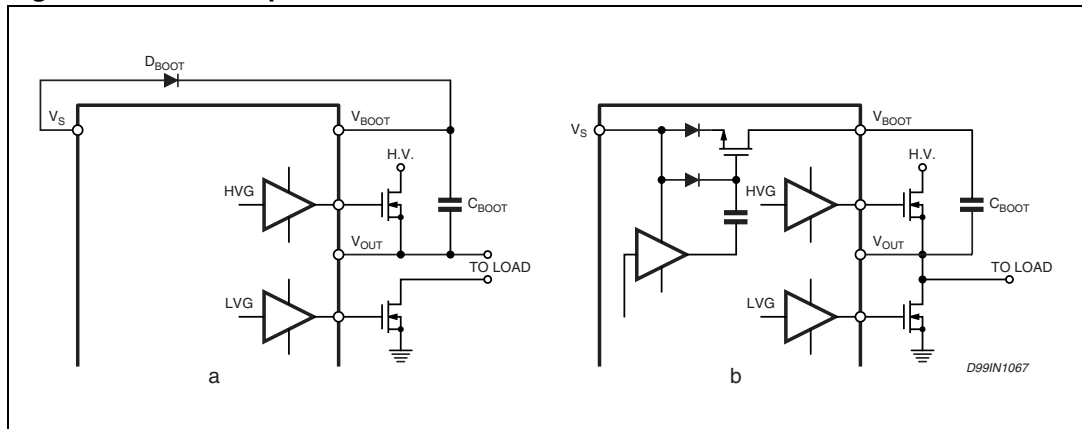


For example: using a power MOS with a total gate charge of 30nC the drop on the bootstrap DMOS is about 1V, if the  $T_{\text{charge}}$  is 5 $\mu\text{s}$ . In fact:

$$V_{\text{drop}} = \frac{30\text{nC}}{5\mu\text{s}} \cdot 125\Omega \sim 0.8\text{V}$$

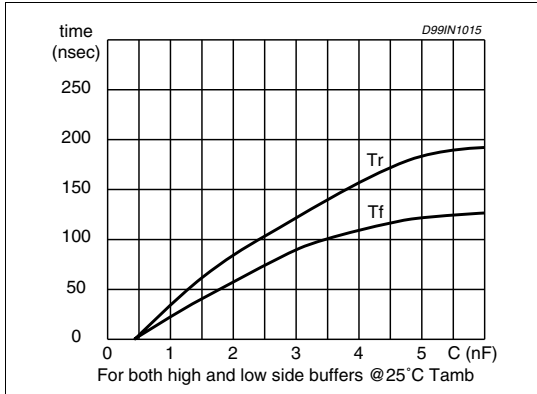
$V_{\text{drop}}$  has to be taken into account when the voltage drop on  $C_{\text{BOOT}}$  is calculated: if this drop is too high, or the circuit topology doesn't allow a sufficient charging time, an external diode can be used.

**Figure 4. Bootstrap driver**

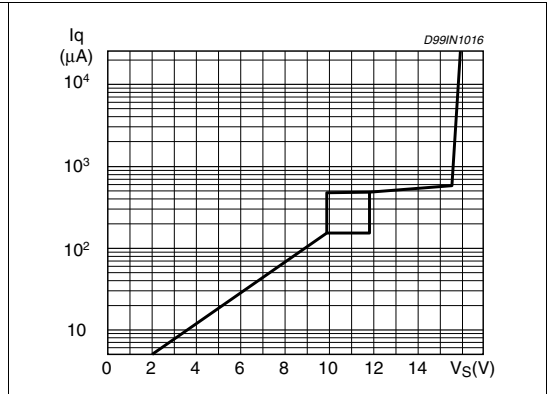


# 5 Typical characteristic

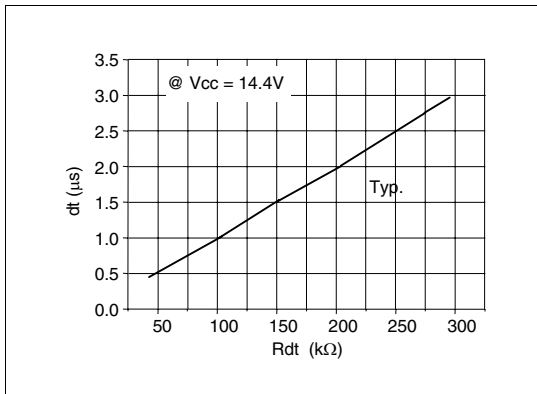
**Figure 5. Typical rise and fall times vs load capacitance**



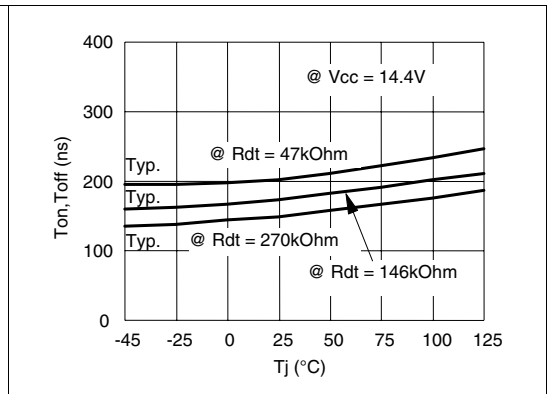
**Figure 6. Quiescent current vs supply voltage**



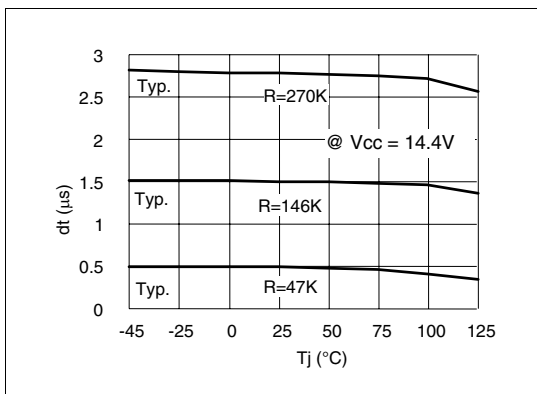
**Figure 7. Dead time vs resistance**



**Figure 8. Driver propagation delay vs temperature**



**Figure 9. Dead time vs temperature**



**Figure 10. Shutdown threshold vs temperature**

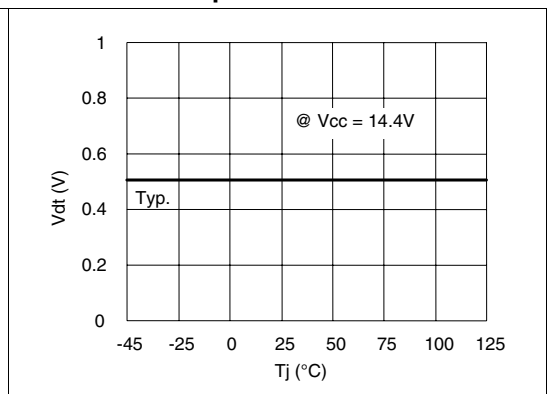


Figure 11. Vcc UV turn On vs temperature

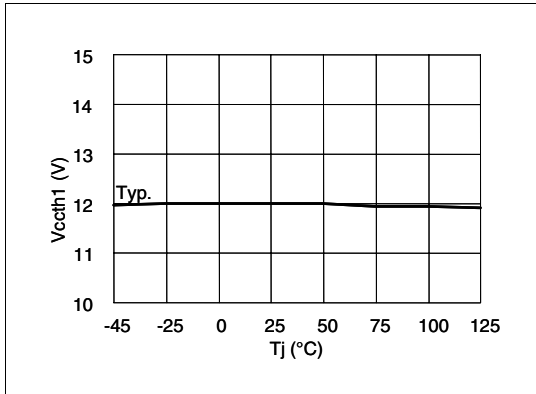


Figure 12. Output source current vs temperature

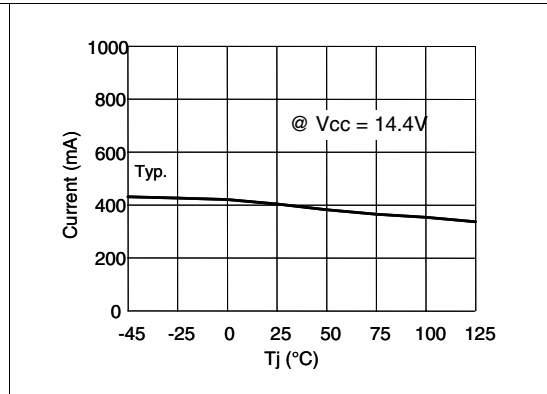


Figure 13. Vcc UV turn Off vs temperature

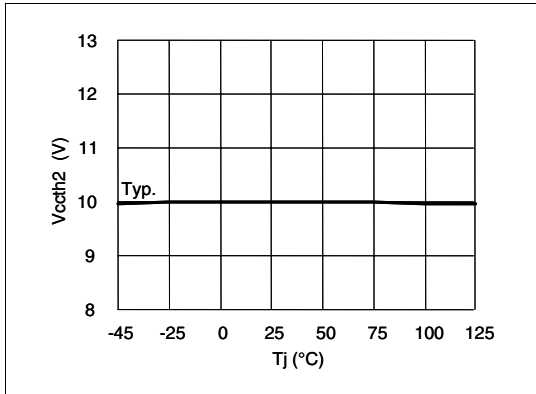
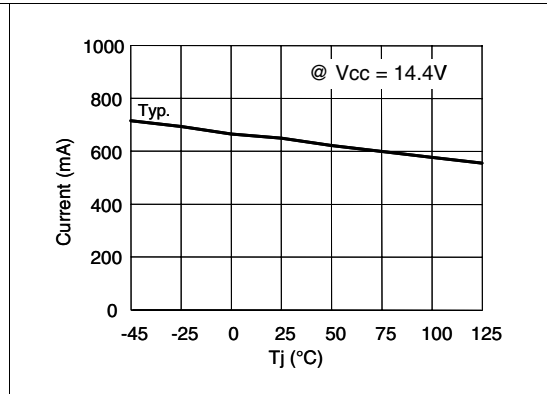


Figure 14. Output sink current vs temperature



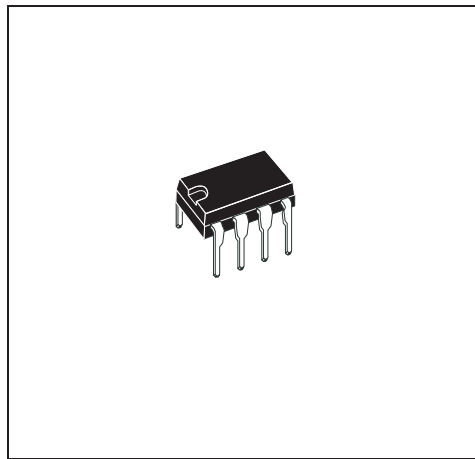
## 6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

Figure 15. DIP-8 mechanical data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
I			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

**OUTLINE AND MECHANICAL DATA**



**DIP-8**

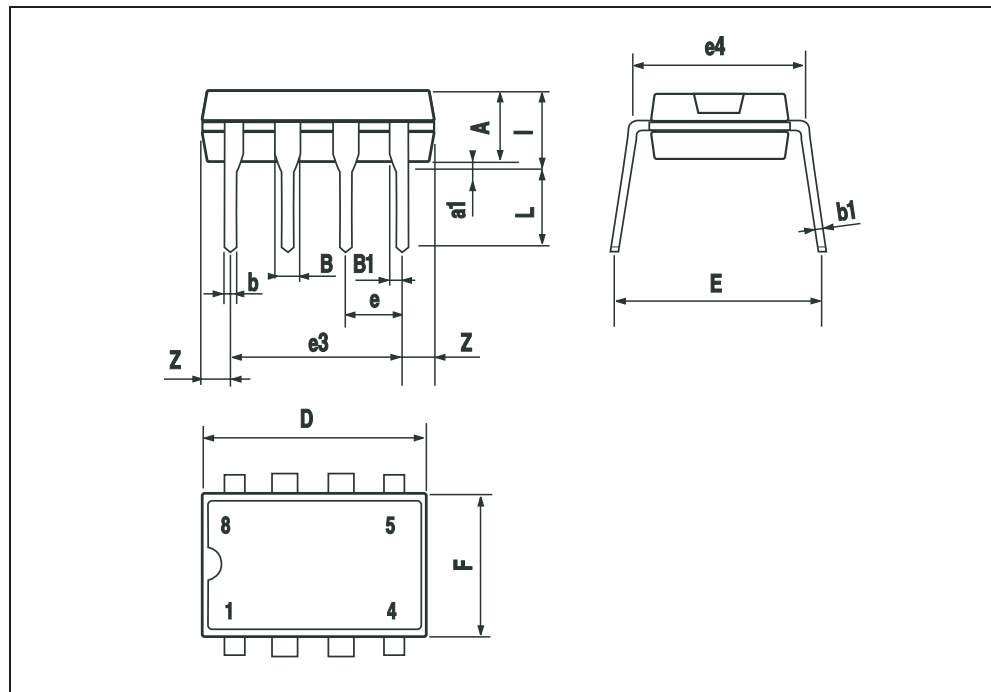
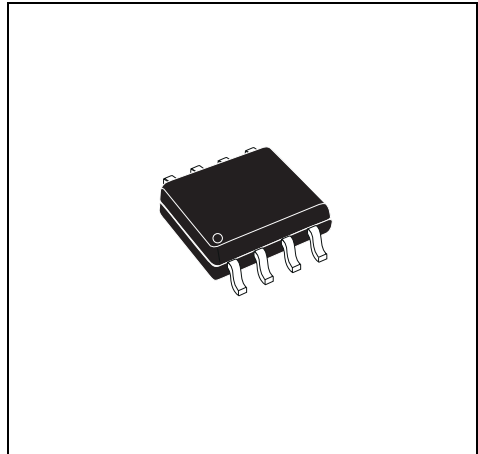


Figure 16. SO-8 mechanical data and package dimensions

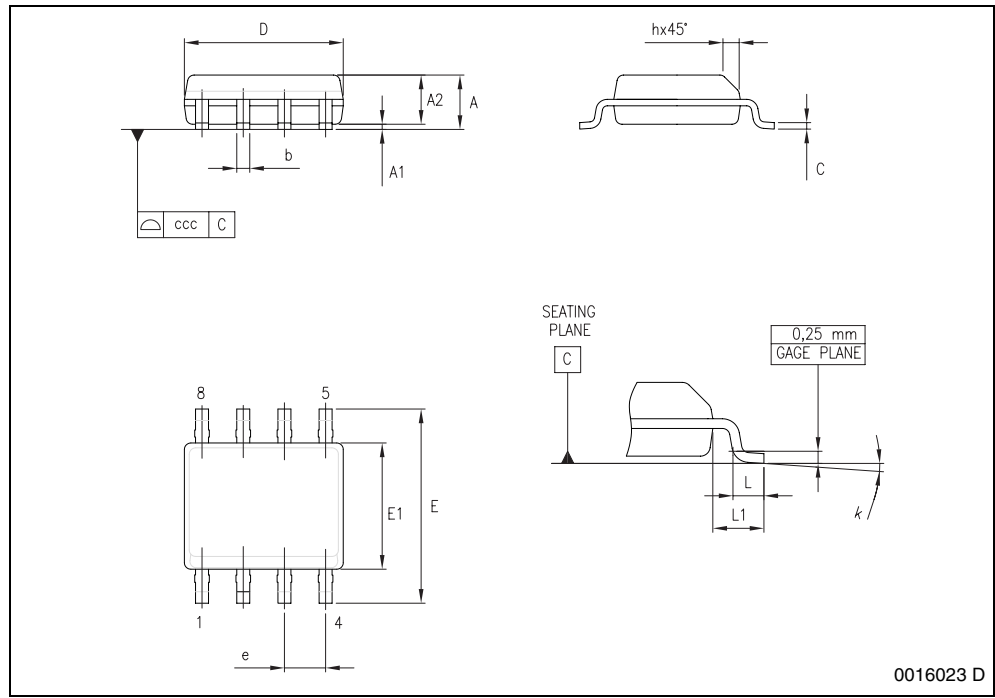
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.750			0.0689
A1	0.100		0.250	0.0039		0.0098
A2	1.250			0.0492		
b	0.280		0.480	0.0110		0.0189
c	0.170		0.230	0.0067		0.0091
D <sup>(1)</sup>	4.800	4.900	5.000	0.1890	0.1929	0.1969
E	5.800	6.000	6.200	0.2283	0.2362	0.2441
E1 <sup>(2)</sup>	3.800	3.900	4.000	0.1496	0.1535	0.1575
e		1.270			0.0500	
h	0.250		0.500	0.0098		0.0197
L	0.400		1.270	0.0157		0.0500
L1		1.040			0.0409	
k	0°		8°	0°		8°
ccc			0.100			0.0039

Notes: 1. Dimensions D does not include mold flash, protrusions or gate burrs.  
 Mold flash, protrusions or gate burrs shall not exceed 0.15mm in total (both side).  
 2. Dimension "E1" does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.

**OUTLINE AND MECHANICAL DATA**



**SO-8**



0016023 D

## 7 Order codes

**Table 7. Order codes**

<b>Part number</b>	<b>Package</b>	<b>Packaging</b>
L6384E	DIP-8	Tube
L6384ED	SO-8	Tube
L6384ED013TR	SO-8	Tape and reel

## 8 Revision history

**Table 8. Document revision history**

Date	Revision	Changes
12-Oct-2007	1	First release



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