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## 16 KEYS OR 8 KEYS TOUCH PAD DETECTOR IC

### GENERAL DESCRIPTION

The TTP229-LSF TonTouch™ IC is capacitive sensing design specifically for touch pad controls. The device built in regulator for touch sensor. Stable sensing method can cover diversity conditions. Human interfaces control panel links through non-conductive dielectric material. The main application is focused at replacing of the mechanical switch or button. The ASSP can independently handle the 8 touch pads or up to 16 touch pads.

### FEATURES

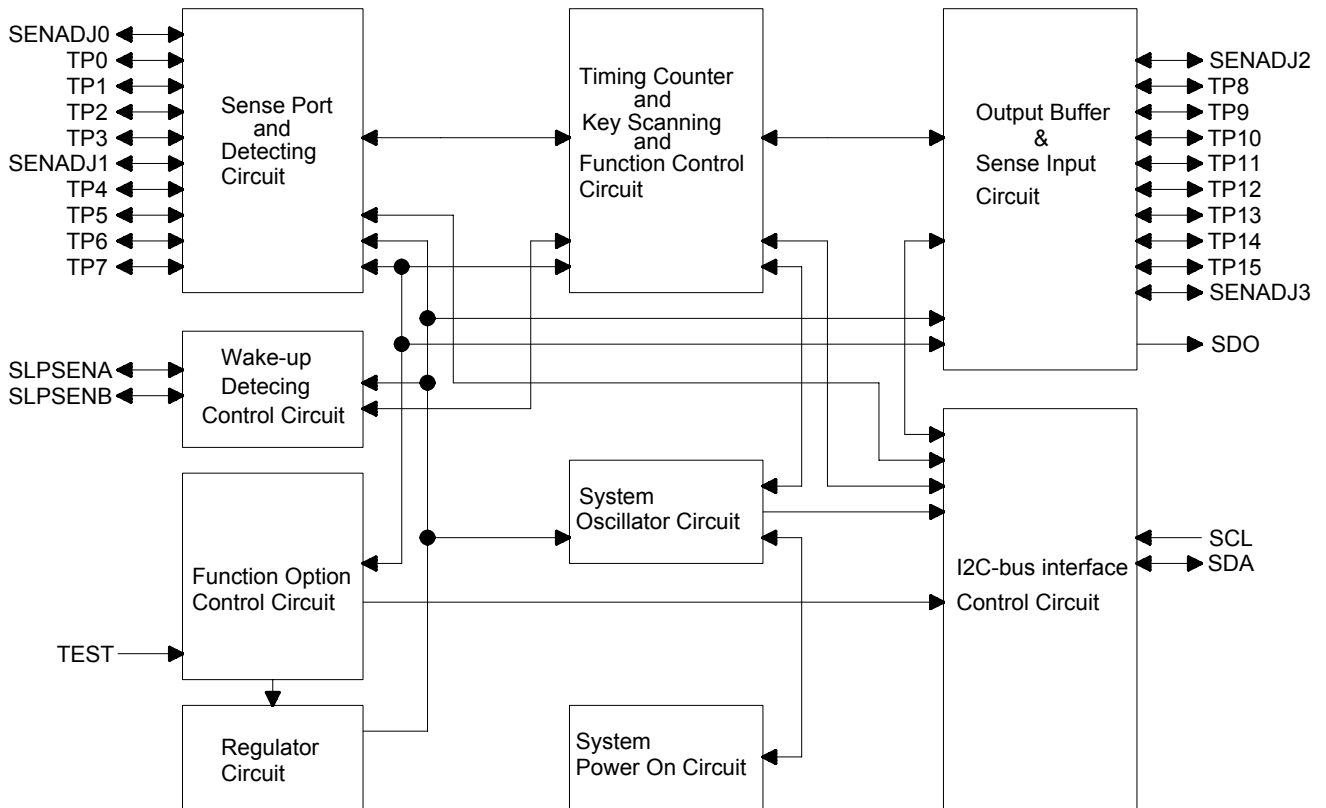
- Operating voltage : 2.4V~5.5V
- Built-in regulator
- Stand-by current  
At 3V, and sleep mode slow sampling rate 8Hz :  
=> Typical 2.5uA for 16 input keys  
=> Typical 2.0uA for 8 input keys
- Provides to set 8 direct keys or 16 direct keys by option
- Provides to set 8 separate outputs only for 8 direct input keys mode
- Has I<sup>2</sup>C-bus slave interface, both can use for 8 and 16 direct input keys mode  
TTP229-LSF Slave Device Identifier and Address => [1010 111R]
- 8 separate outputs can select output driving types by option  
(CMOS/OD/OC with active high/low)
- Offer multi-key or single-key feature by option
- Provides two kinds of sampling rate that slow sampling rate 8Hz  
and fast sampling rate 64Hz at sleep mode
- Have the maximum key-on time about 80sec by pin option
- Sensitivity can adjust by the capacitance(1~50pF) outside
- After power-on have about 0.5sec stable-time,  
During the time do not touch the key pad, and all functions are disabled
- Auto calibration for environment changing  
And the re-calibration period is about 4.0sec, when all keys are not activated for fixed time

### APPLICATION

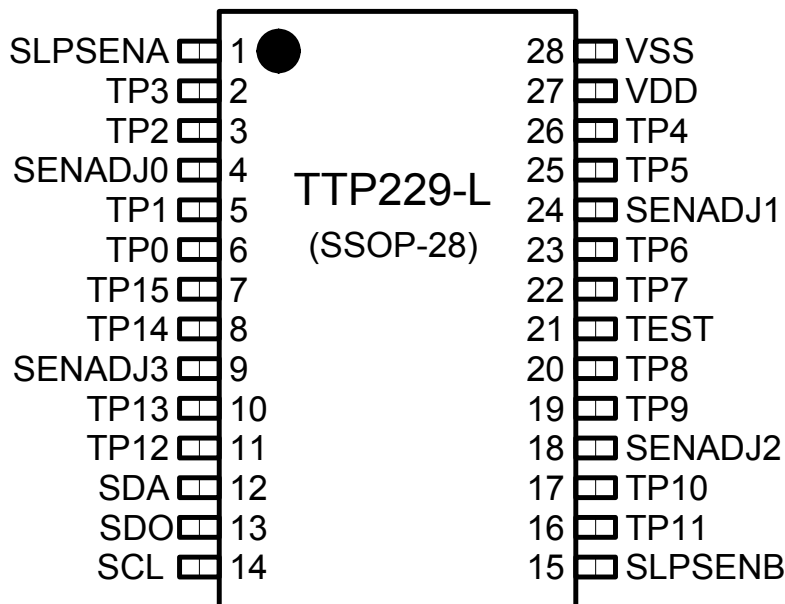
- Wide consumer products
- Button key replacement



## BLOCK DIAGRAM



## PACKAGE CONFIGURATION



**PIN DESCRIPTION**

Pin No.	Pin Name	Share Pin	I/O Type	Pin Description
1	SLPSENA		I/O	Sleep mode sensitivity adjustment pin for group-A(TP0~7)
2	TP3	SKMS1	I/O	Touch pad input pin(KEY-3) Key action function option-1(Single-key/Multi-key) Default is all single-key
3	TP2	KYSEL	I/O	Touch pad input pin(KEY-2) Key number function option(8-keys/16-keys) Default is 8-keys
4	SENADJ0		I/O	Touch pad TP0~3 sensitivity adjust common pin
5	TP1	SAHL	I/O	Touch pad input pin(KEY-1) Output type function option(Active High/Low) Default is active-high for TPQ0~7
6	TP0	OPDEN	I/O	Touch pad input pin(KEY-0) Output type function option(CMOS/OD/OC for 8-keys) Default is CMOS
7	TP15	TPQ7	I/O/OD	Touch pad input pin(KEY-15) 8-keys direct output pin(TPQ7)
8	TP14	TPQ6	I/O/OD	Touch pad input pin(KEY-14) 8-keys direct output pin(TPQ6)
9	SENADJ3		I/O	Touch pad TP12~15 sensitivity adjust common pin
10	TP13	TPQ5	I/O/OD	Touch pad input pin(KEY-13) 8-keys direct output pin(TPQ5)
11	TP12	TPQ4	I/O/OD	Touch pad input pin(KEY-12) 8-keys direct output pin(TPQ4)
12	SDA		I/OD	Data pin for the I <sup>2</sup> C-bus serial data interface
13	SDO		O	Data valid signal output, option active Low/High by TP1
14	SCL		I	Serial clock input pin for the I <sup>2</sup> C-bus serial interface
15	SLPSENB		I/O	Sleep mode sensitivity adjustment pin for group-B(TP8~15)
16	TP11	TPQ3	I/O/OD	Touch pad input pin(KEY-11) 8-keys direct output pin(TPQ3)
17	TP10	TPQ2	I/O/OD	Touch pad input pin(KEY-10) 8-keys direct output pin(TPQ2)
18	SENADJ2		I/O	Touch pad TP8~11 sensitivity adjust common pin
19	TP9	TPQ1	I/O/OD	Touch pad input pin(KEY-9) 8-keys direct output pin(TPQ1)
20	TP8	TPQ0	I/O/OD	Touch pad input pin(KEY-8) 8-keys direct output pin(TPQ0)



Pin No.	Pin Name	Share Pin	I/O Type	Pin Description
21	TEST		I-PL	Only for test
22	TP7	SKSRT	I/O	Touch pad input pin(KEY-7) Maximum key-on time function option(Infinite/80sec) Default is infinite
23	TP6	SLWPTM	I/O	Touch pad input pin(KEY-6) Sleep mode sampling length function option(4.0/2.0mS) Default is 4.0ms
24	SENADJ1		I/O	Touch pad TP4~7 sensitivity adjust common pin
25	TP5	WPSCT	I/O	Touch pad input pin(KEY-5) Sampling rate at sleep mode function option(8Hz/64Hz) Default is 8Hz
26	TP4	SKMS0	I/O	Touch pad input pin(KEY-4) Key action function option-0(Single-key/Multi-key) Default is all single-key
27	VDD		P	Positive power supply
28	VSS		P	Negative power supply, ground

**Note : Pin Type**

I =&gt; CMOS input only

I-PH =&gt; CMOS input and pull-high resister

I-PL =&gt; CMOS input and pull-low resister

O =&gt; CMOS push-pull output

I/O =&gt; CMOS I/O

P =&gt; Power / Ground

OD =&gt; CMOS open drain output

(For OD TPQ0~TPQ7 pins have Diode protective circuit, SDA pin has no Diode protective circuit)

**ELECTRICAL CHARACTERISTICS****• Absolute Maximum Ratings**

Parameter	Symbol	Conditions	Value	Unit
Operating Temperature	T <sub>OP</sub>	—	-40 ~ +85	°C
Storage Temperature	T <sub>STG</sub>	—	-50 ~ +125	°C
Power Supply Voltage	VDD	T <sub>a</sub> =25°C	VSS-0.3 ~ VSS+6.0	V
Input Voltage	V <sub>IN</sub>	T <sub>a</sub> =25°C	VSS-0.3 to VDD+0.3	V
Human Body Mode	ESD	—	6	KV

Note : VSS symbolizes for system ground

**• DC/AC Characteristics** : (Test condition at room temperature=25°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
<b>Operating Voltage</b>	VDD		2.4	-	5.5	V
<b>Internal Regulator Output</b>	VREG		2.2	2.3	2.4	V
<b>Operating Current</b> (no load)	I <sub>OP</sub>	VDD=3.0V		20		uA
<b>Stand-by Current</b> (VDD=3.0V) (Sampling length 4.0mS)	I <sub>SD</sub>	Sampling rate 8Hz	Set 8-Keys	2.0		uA
			Set 16-Keys	2.5		
		Sampling rate 64Hz	Set 8-Keys	5.5		
			Set 16-Keys	9.0		
<b>Input Ports</b>	V <sub>IL</sub>	Input Low Voltage	0	-	0.2	VDD
<b>Input Ports</b>	V <sub>IH</sub>	Input High Voltage	0.8	-	1.0	VDD
<b>Output Port Sink Current</b>	I <sub>OL</sub>	VDD=3V, V <sub>OL</sub> =0.6V	-	8	-	mA
<b>Output Port Source Current</b>	I <sub>OH</sub>	VDD=3V, V <sub>OH</sub> =2.4V	-	-4	-	mA
<b>Wake-up Response Time</b> (at sleep mode)	T <sub>WU</sub>	VDD=3V, Sampling rate 8Hz		125		mS
		VDD=3V, Sampling rate 64Hz		15.6		mS
<b>Output Response Time</b> (at operation)	T <sub>R</sub>	VDD=3V, set 16-keys		32		mS
		VDD=3V, set 8-keys		16		mS
<b>Maximum Key-on Time</b>	T <sub>MOT</sub>		50	80	110	Sec
<b>Input Pin Pull-low Resistor</b> (TEST)	R <sub>PL</sub>	VDD=3V,		30K		ohm



### FUNCTION DESCRIPTION

#### 1. Sensitivity adjustment

The total loading of electrode size and capacitance of connecting line on PCB can affect the sensitivity. So the sensitivity adjustment must according to the practical application on PCB. The TTP229-LSF offers some methods for adjusting the sensitivity outside.

##### 1-1 by the electrode size

Under other conditions are fixed. Using a larger electrode size can increase sensitivity. Otherwise it can decrease sensitivity. But the electrode size must use in the effective scope.

##### 1-2 by the panel thickness

Under other conditions are fixed. Using a thinner panel can increase sensitivity. Otherwise it can decrease sensitivity. But the panel thickness must be below the maximum value.

##### 1-3 by the value of external capacitor (please see the down Figure 1-3-1)

Under other conditions are fixed. When adding the values of CJ0~CJ3 and CJWA and CJWB will reduce sensitivity in the useful range ( $1pF \leq CJ0 \sim CJ3 \leq 50pF$ ,  $1pF \leq CJWA \sim CJWB \leq 50pF$ ).

When do not use any capacitor that means open on the position of capacitor, the sensitivity is most sensitive. The capacitors CJ0~CJ3 are used to adjust the sensitivity of keys at operation mode.

The capacitors CJWA and CJWB are used to adjust the Wake-up sensitivity at sleep mode.

About the relation of capacitor and controlled keys please to see below table.

The capacitor	The keys-group controlled and adjusted
CJ0	K0~K3 group
CJ1	K4~K7 group
CJ2	K8~K11 group
CJ3	K12~K15 group
CJWA	K0~K7 group
CJWB	K8~K15 group

Note : When using the value of capacitor to adjust the sensitivity, recommending to adjust the CJ0~CJ3 capacitor for K0~K15 first, then adjusting the CJWA and CJWB capacitor for Wake-up sensitivity.

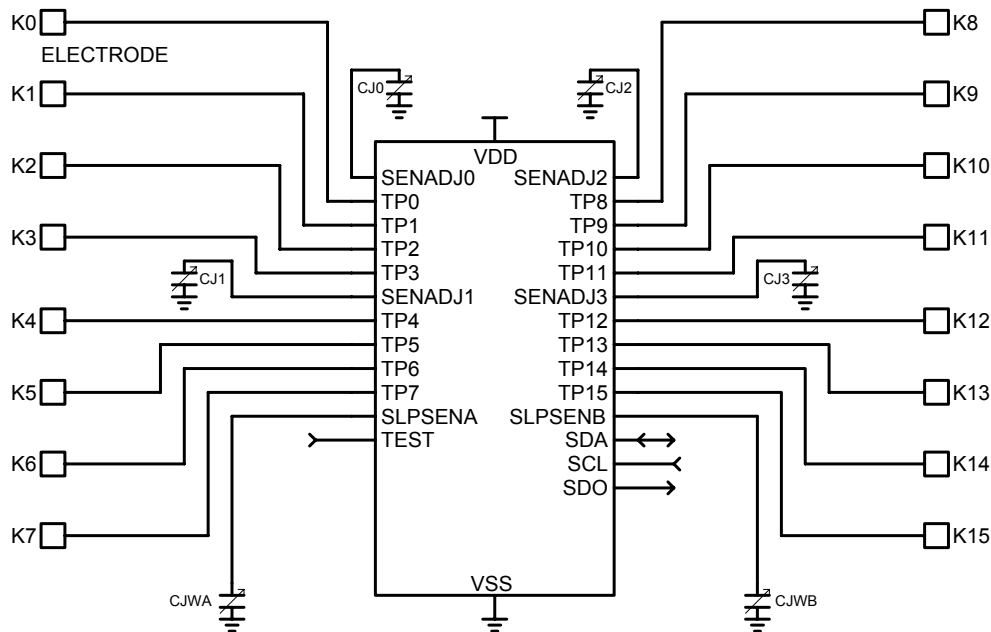


Figure 1-3-1



### 2. Input keys number select

The TTP229-LSF has 8 keys input mode and 16 keys input mode. These modes are selected via high-value resistor connected to the TP2(KYSEL) pin to VSS, or not. The default that TP2(KYSEL) pin is not used resistor connected to VSS is selected 8 keys input mode. Another is selected 16 keys input mode that has used a high-value resistor connected to VSS.

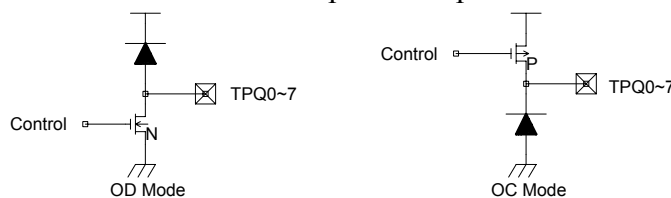
### 3. Output mode

The TTP229-LSF has 8 pins direct output mode and I<sup>2</sup>C-bus slave interface mode. The output of 16 keys input mode only offer I<sup>2</sup>C-bus slave interface. The 8 keys input mode has two kinds of output that 8 pins direct output and I<sup>2</sup>C-bus slave interface. The 8 pins direct output only use at 8 keys input mode.

3-1 At the 8 pins direct output mode, the TTP229-LSF has two kinds of output type that they are CMOS type output and OD (Open Drain) type output. These are selected by the TP0(OPDEN) pin. The CMOS type output is default that the TP0(OPDEN) pin is not used any component to VSS. When the TP0(OPDEN) pin is used a high-value resistor connected to VSS, it is selected OD type output.

3-2 When selecting 8 pins direct CMOS output mode, the output channels can be set active-high or active-low by TP1(SAHL) pin. The default that the TP1(SAHL) pin is not used a high-value resistor, it is set active-high. When the TP1(SAHL) pin has a high-value resistor connected to VSS, it is set active-low.

3-3 At 8 pins direct OD output mode, it has OD (Open Drain) or OC (Open collector) output mode to be selected by the TP1(SAHL) pin. The TP1(SAHL) pin has a high-value resistor connected to VSS, it is selected OC mode. Another it is selected OD mode that does not has a resistor. The default is OD mode. The states of OD mode are floating and active-low. And the states of OC mode are floating and active-high. The structure of OD and OC output mode please to see the below figure.



Note : the output pins have Diode protective circuit in the chip. So when it selected OD or OC mode. Do not propose to connect other device that uses the different voltage. That avoids to occurring the leakage current in the system.



3-4 At I<sup>2</sup>C-bus slave interface mode the SDA pin is a serial data pin, the SCL is a serial clock input pin. The SDA and SCL pins must be pulled-high with an external resistor.

And the 4-bits identify code for the TTP229-LSF is " (1010) ". The device address for TTP229-LSF B3~B1 bits are fixed " 111 ". The TTP229-LSF 8-bits slave device address includes 4-bits identifier, 3-bits address and R/W bit (see the Table 3-4-1).

The TTP229-LSF IC uses the I<sup>2</sup>C-bus slave interface data transmission protocol to output the data of the touch pads (TP0~TP15 pins), so the TTP229-LSF only accepts the read operation that R/W bit is " 1 ". If it is " 0 ", the TTP229-LSF will not respond the write operation. Otherwise, the I<sup>2</sup>C-bus slave interface of TTP229-LSF conforms to the communication protocols. It supports the fast mode that the maximum SCL clock frequency is 400KHz.

The I<sup>2</sup>C-bus slave interface supports the following communication protocols:

Bus not busy : The SDA and the SCL lines remain High level when the bus is not active.

Start condition : Start condition is SDA 1 to 0 transition when SCL=1.(see figure 3-4-2)

Stop condition : Stop condition is SDA 0 to 1 transition when SCL=1.(see figure 3-4-2)

Data valid : Following a start condition, the data on the SDA line must be stable during the High period of SCL. The High or Low state of the data line can only change when the clock signal on the SCL line is Low.(see figure 3-4-2)

ACK (Acknowledge) : An ACK signal indicates that a data transfer is completed successfully. The transmitter (the master or the slave) releases the bus after transmitting eight bits. During the ninth clock, which the master generates, the receiver pulls the SDA line low to acknowledge that it successfully received the eight bits of data. But the slave does not send an ACK if it does not successfully received the eight bits of data.

In data read operations, the slave releases the SDA line after transmitting 8 bits of data and then monitors the line for an ACK signal during the ninth clock period. If an ACK is detected, the slave will continue to transmit next data. If an ACK is not detected, the slave terminates data transmission and waits for a stop condition to be issued by the master before returning to its stand-by mode.

Slave Address : The identify code for the TTP229-LSF is " (1010) ". The device address B3 , B2 and B1 are fixed " 111 " .

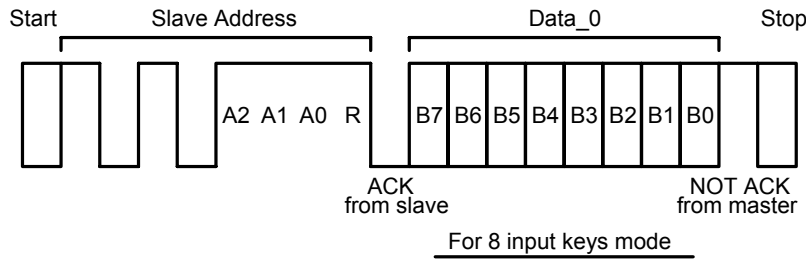
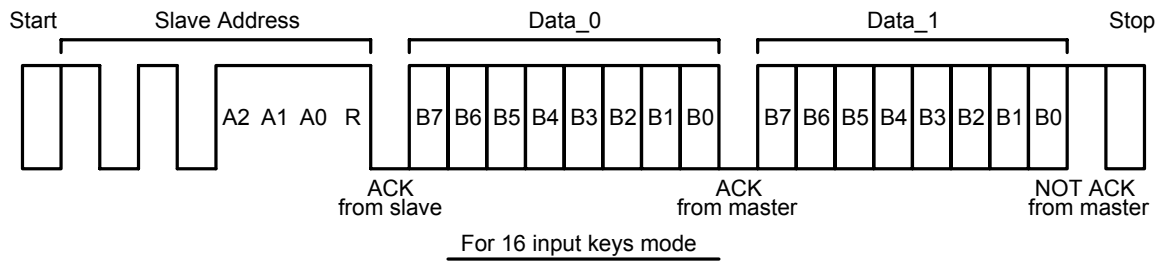
Read/Write : The final (eighth) bit of the slave address defines the type of operation to be performed. If the R/W bit is " 1 " , a read operation is executed. If it is " 0 " , a write operation is executed. But the TTP229-LSF only accepts read operation.

The sequence of read data operation please see figure 3-4-1.

Table 3-4-1. Slave Device Addressing

Device	Device Identifier				Device Address			R/W Bit
	B7	B6	B5	B4	B3	B2	B1	B0
TTP229-LSF	1	0	1	0	1	1	1	R





Note : Data\_0 : B7~B0 is TP0~TP7 on/off status. 0 is key off, 1 is key on.  
 Data\_1 : B7~B0 is TP8~TP15 on/off status. 0 is key off, 1 is key on.

Figure 3-4-1. Read Operation Sequence

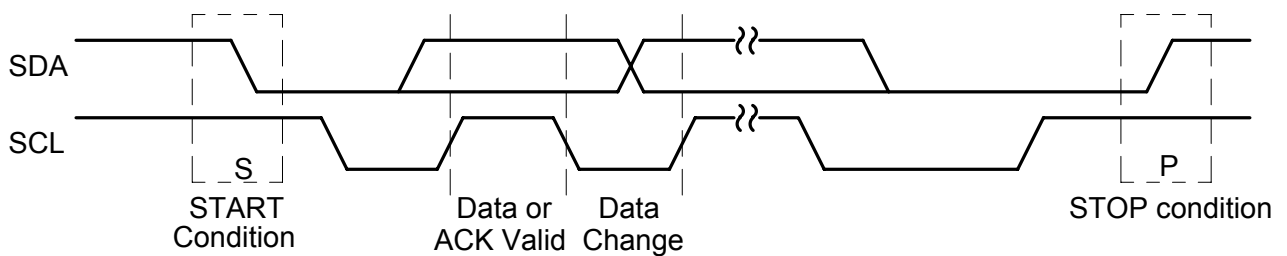


Figure 3-4-2. Data Transmission Sequence

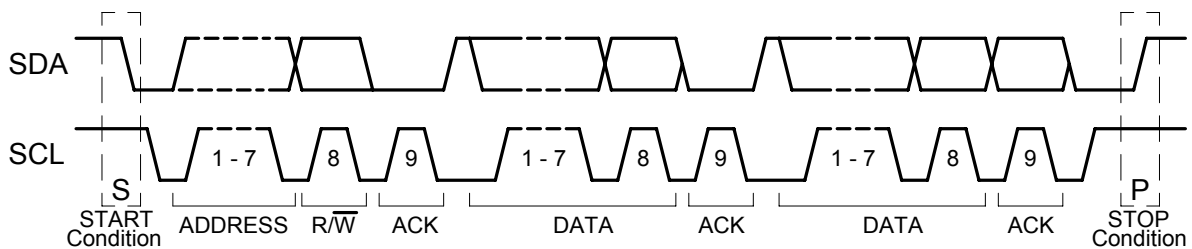


Figure 3-4-3. A complete data transfer

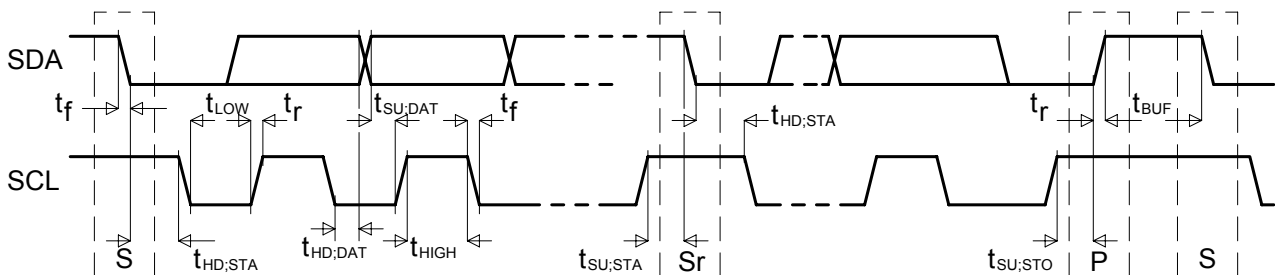


Figure 3-4-4. Definition of timing for F/S-mode devices on the I<sup>2</sup>C-bus

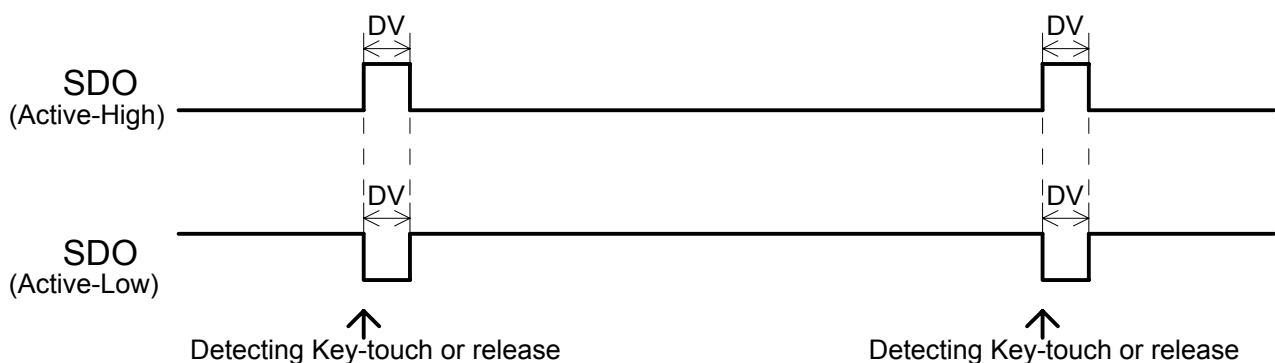
Table 3-4-2. Characteristics of the SDA and SCL bus lines for F/S-mode I<sup>2</sup>C-bus devices

Parameter	Symbol	Standard-Mode		Fast-Mode		Unit
		Min.	Max.	Min.	Max.	
SCL clock frequency	$f_{SCL}$		100		400	KHz
LOW period of the SCL clock	$t_{LOW}$	4.7		1.3		us
HIGH period of the SCL clock	$t_{HIGH}$	4.0		0.6		us
Hold time (repeated) START condition	$t_{HD;STA}$	4.0		0.6		us
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7		0.6		us
Data hold time	$t_{HD;DAT}$	0		0		us
Data set-up time	$t_{SU;DAT}$	250		100		ns
Rise time of both SDA and SCL signals	$t_r$		1000		300	ns
Fall time of both SDA and SCL signals	$t_f$		300		300	ns
Set-up time for STOP condition	$t_{SU;STO}$	4.0		0.6		us
Bus free time between a STOP and START condition	$t_{BUF}$	4.7		1.3		us
Capacitive load for each bus line	$C_b$		400		400	pF

### 3-5. Data valid (DV) signal output

The TTP229-LSF can output the Data Valid signal (DV pulse) by SDO pin, when the state of any key (TP0~TP15) has been detected change at the normal operation mode. It can be used to trigger other devices. And it can be set active high or low by TP1(SAHL) pin. The default is active-low that TP1(SAHL) pin is not used resistor connected to VSS. Another it is active-high. The typical value of DV pulse width is 93us. About the DV pulse please see the below figure.

When the system for TTP229-LSF is set to use the maximum key-on time enable function, and key detected touch and kept over the timer (about 80sec), the TTP229-LSF will return to the power-on initial state, and the key state becomes inactive until the next detection. At the time key state has change, but the SDO pin does not output the DV pulse. The point needs to attend.



DV pulse width Typ. = 93us.



#### 4. Key operating mode

The TTP229-LSF has the Single-key and Multi-key functions. These functions are set by TP3(SKMS1) and TP4(SKMS0) pins. The all 16 keys can use one group, or the 16 keys can distributed into two groups. The group-1 includes TP0, TP1, TP2, TP3, TP8, TP9, TP10, TP11 keys. The group-2 includes TP4, TP5, TP6, TP7, TP12, TP13, TP14, TP15 keys. How to set the function? Please see below table 4-1 :

Table 4-1. The functions of TP3(SKMS1) and TP4(SKMS0) option

TP3 (SKMS1)	TP4 (SKMS0)	Operating function
1	1	All Single-keys : one group(16keys)
1	0	Two groups operate : group-1=>Single key ; group-2=>Single key
0	1	Two groups operate : group-1=>Single key ; group-2=>Multi key
0	0	All Multi-keys : one group(16 keys)

Note : 1. One group : TP0~TP15.

Two groups : Group-1=>TP0,TP1,TP2,TP3,TP8,TP9,TP10,TP11.

Group-2=>TP4,TP5,TP6,TP7,TP12,TP13,TP14,TP15.

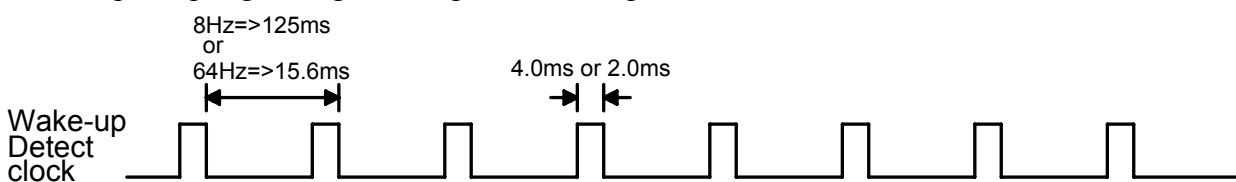
- When uses 8 input keys mode. The using keys are TP0~TP7.
- The option states of TP3 and TP4, the "0" state is used a high-value resistor connected to VSS, the "1" state is not used resistor connected to VSS.
- The key detection acknowledges in Single-key function, the priority is by the key scanning order (from TP0 to TP15) when many keys are touched effectively. It is not by the key touching strength.

#### 5. Wake-up sampling rate and sampling length at sleep mode

The TTP229-LSF has two kinds of sampling rate at sleep mode. These are 8Hz and 64Hz. The two functions are selected by TP5(SLWPTM) pin. The TP5(SLWPTM) pin has used a high-value resistor connected to VSS, it selected the 64Hz sampling rate. Another it is 8Hz that is not used resistor connected to VSS. The 8Hz sampling is the default.

And TTP229-LSF has two kinds of sampling length at sleep mode. They are 4ms and 2ms that are selected by TP6(WPSCT) pin. The default is 4ms that TP6(WPSCT) pin is not used resistor connected to VSS. Another it is 2ms that TP6 pin has used a high-value resistor connected to VSS.

Wake-up sampling timing and length in the sleep mode :



**6. Maximum key-on time**

If some objects cover in the sense pad, and causing the change quantity enough to be detected. To prevent this, the TTP229-LSF sets a timer to monitor the detection. The timer is the maximum key-on time. It is set about 80sec at 3V. When the detection is over the timer, the system will return to the power-on initial state, and the output becomes inactive until the next detection. The function is set via a high-value resistor connected to the TP7(SKSRT) pin to VSS. The TP7(SKSRT) pin does not has the resistor, it is set disable the maximum key-on time, then the key acts infinitely, this is the default. Another it is set enable the maximum key-on time that has a resistor.

**7. Built-in regulator**

The capacitive sensing touch pad IC needs stable power. So the TTP229-LSF built in regulator in the chip. It can make the internal power to keep up steady. And the sensitivity detection is normal for chip. And the stable power can avoid sensitivity anomalies and false detections.

**8. Auto calibration function**

The TTP229-LSF includes a full auto-calibration function. After the device is powered-on, it will calibrate the initial condition of environment first. On the duration time all the functions are disabled, so do not operate. Then the system is into stand-by mode. And all keys are not detected touch more than about 4 seconds, then the system do re-calibration automatically. The procedure is fixed and repeated. By implementing this feature the system can catch the conditions of environment changing. And let operation of the system is normal.



9. The timing from sleep mode to operation mode

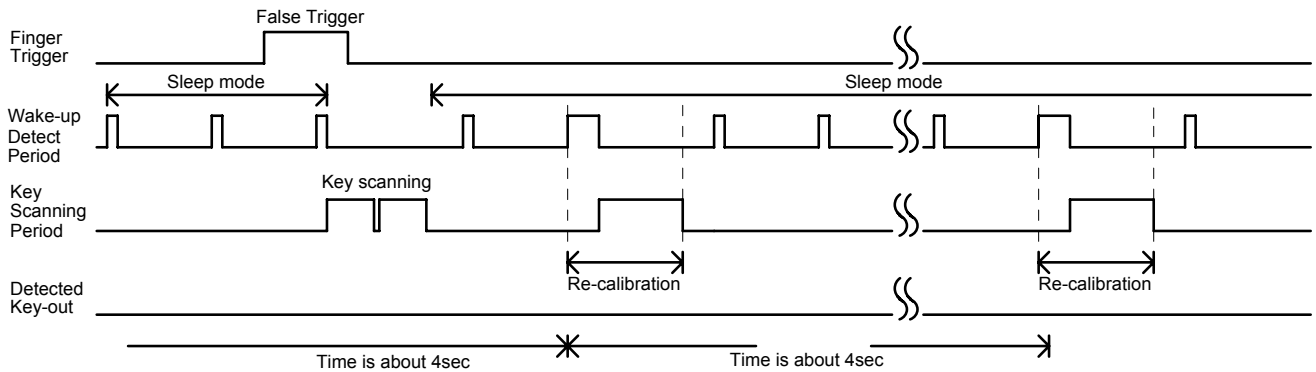


Figure 9-1. The timing for false trigger

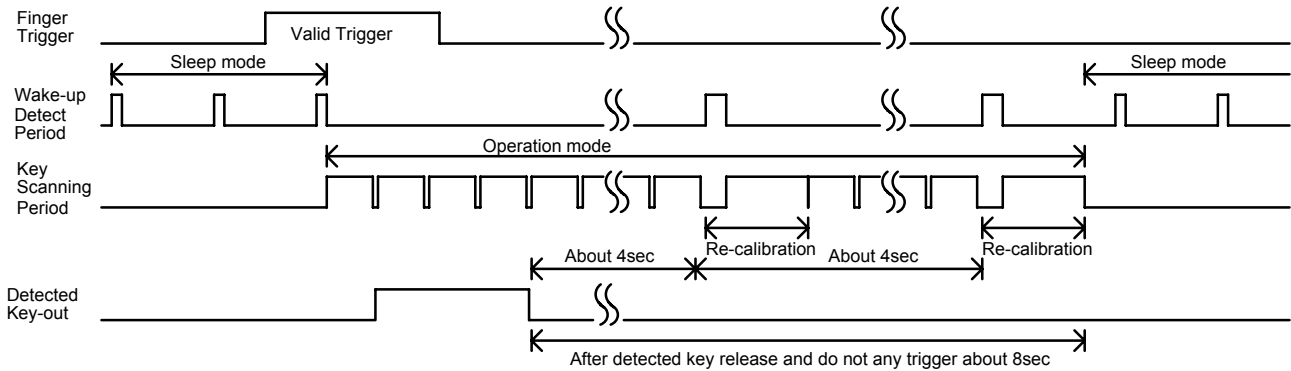


Figure 9-2. The timing for valid trigger

**10. Option table****Option table :**

Option pin	Option states		Feature	Remark
TP0 (OPDEN)	TP0 (OPDEN)	TP1 (SAHL)	8 output pins => CMOS output active-high 2-wires serial interface => CMOS output active-low	Default
	1	1		
TP1 (SAHL)	1	0	8 output pins => CMOS output active-low 2-wires serial interface => CMOS output active-high	
	0	1	8 output pins => OD output active-low 2-wires serial interface => CMOS output active-low	
TP2 (Kysel)	0	0	8 output pins => OC output active-high 2-wires serial interface => CMOS output active-high	
	1		8 input keys mode	Default
TP3 (SKMS1)	0		16 input keys mode	
	TP3 (SKMS1)	TP4 (SKMS0)	All Single-keys : one group(16keys)	Default
1	1			
TP4 (SKMS0)	1	0	Two groups operate : group-1=>Single key ; group-2=>Single key	
	0	1	Two groups operate : group-1=>Single key ; group-2=>Multi key	
TP5 (WPSCT)	0	0	All Multi-keys : one group(16 keys)	
	1		8Hz sampling rate for wake-up in sleep mode	Default
TP6 (SLWPTM)	0		64Hz sampling rate for wake-up in sleep mode	
	1		Wake-up sampling length=>about 4.0ms	Default
TP7 (SKSRT)	0		Wake-up sampling length=>about 2.0ms	
	1		Maximum key-on time disable=>infinite	Default
	0		Maximum key-on time enable=>about 80sec	

Note : 1. About the combinations of group-1 and group-2, please see above point-4.

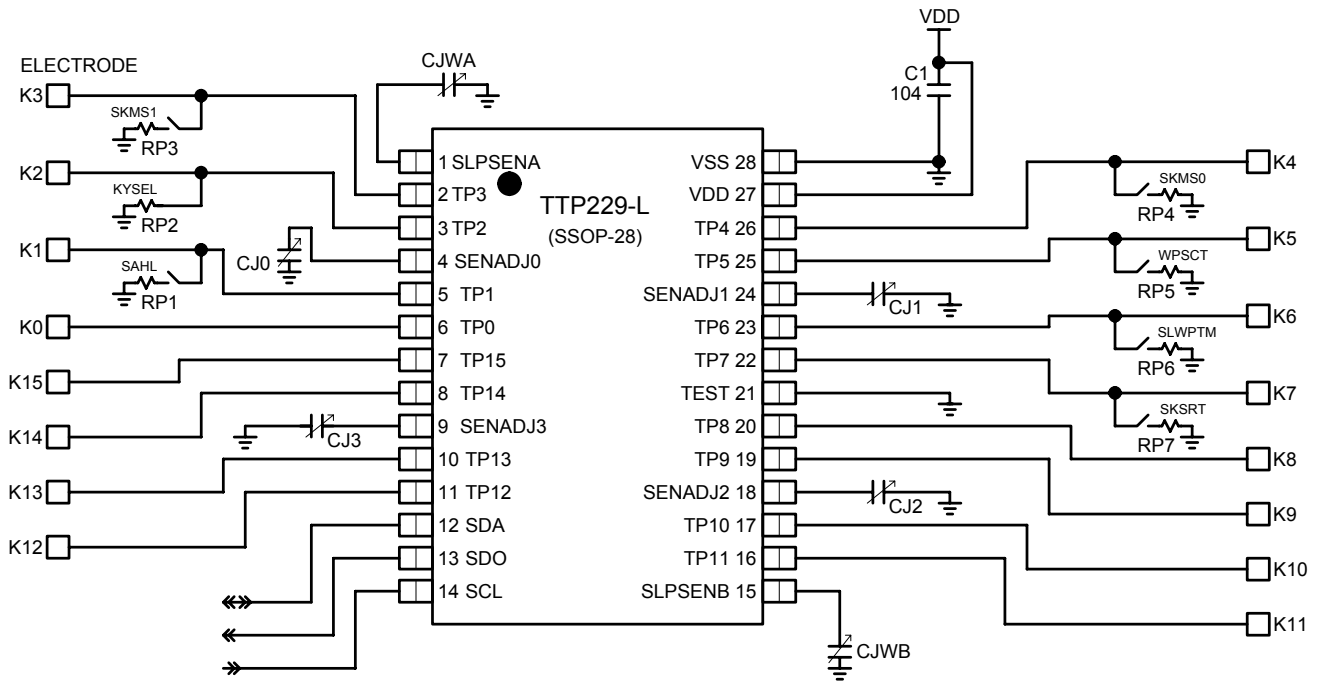
2. Option states "1" mean internal pull-up (default).

3. Option states "0" mean that TP0~TP7 pins are via high-value resistors connected to VSS.



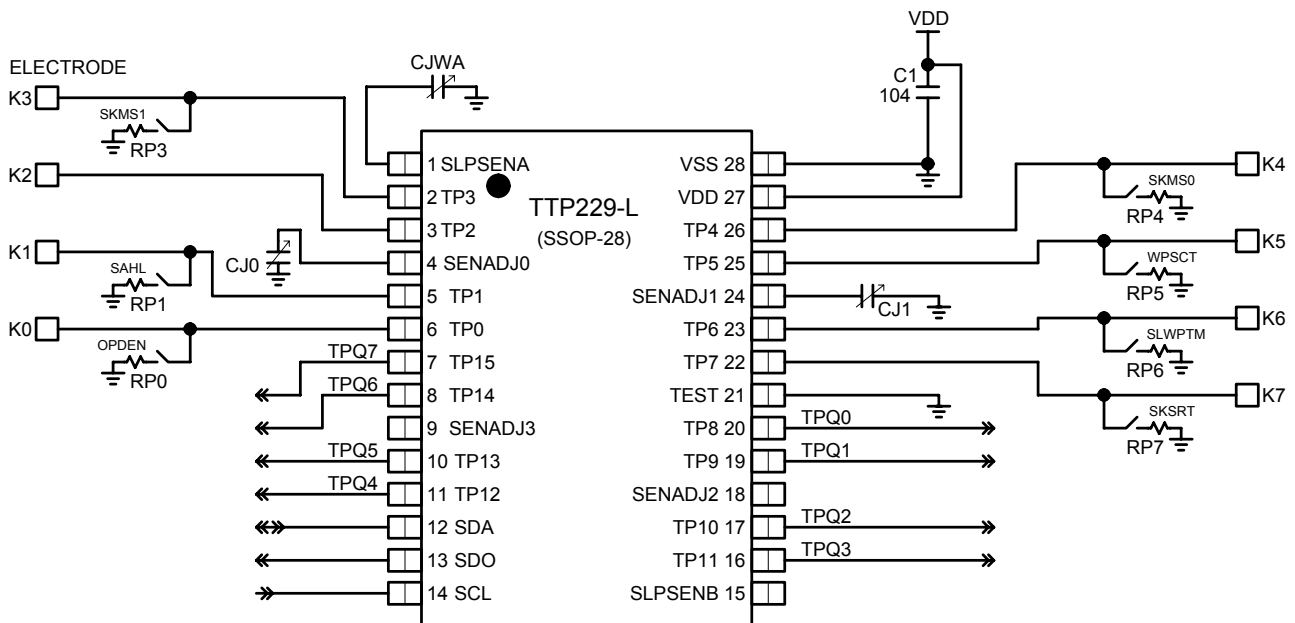
APPLICATION CIRCUIT

APPLICATION FOR 16 INPUT KEYS





## APPLICATION FOR 8 INPUT KEYS



- PS : 1. On PCB, the length of lines from touch pad to IC pin shorter is better.  
And the lines do not parallel and cross with other lines.
- The power supply must be stable. If the supply voltage drift or shift quickly, maybe causing sensitivity anomalies or false detections.
  - The material of panel covering on the PCB can not include the metal or the electric element. The paints on the surfaces are the same.
  - The C1 capacitor must be used between VDD and VSS; and should be routed with very short tracks to the device's VDD and VSS pins (TTP229-LSF).
  - The capacitance CJ0~CJ3 and CJWA~CJWB can be used to adjust the sensitivity. The value of capacitors use smaller, then the sensitivity will be better. The sensitivity adjustment must according to the practical application on PCB. The range value of capacitors are  $1\text{pF} \leq \text{CJ0} \sim \text{CJ3} \leq 50\text{pF}$ ,  $1\text{pF} \leq \text{CJWA} \sim \text{CJWB} \leq 50\text{pF}$ . Recommend to adjust the CJ0~CJ3 capacitor for K0~K15 first, then adjusting the CJWA and CJWB capacitor for Wake-up sensitivity.
  - The sensitivity adjustment capacitors (CJ0~CJ3, CJWA~CJWB) must use smaller temperature coefficient and more stable capacitors. Such are X7R, NPO for example. So for touch application, recommend to use NPO capacitor, for reducing that the temperature varies to affect sensitivity.
  - Recommend to use 820K ohm resistor for RP0~RP7 resistors.
  - When the system does not use the serial output interface, the SCL pin must be connected to VSS or VDD, it is not allowed floating.

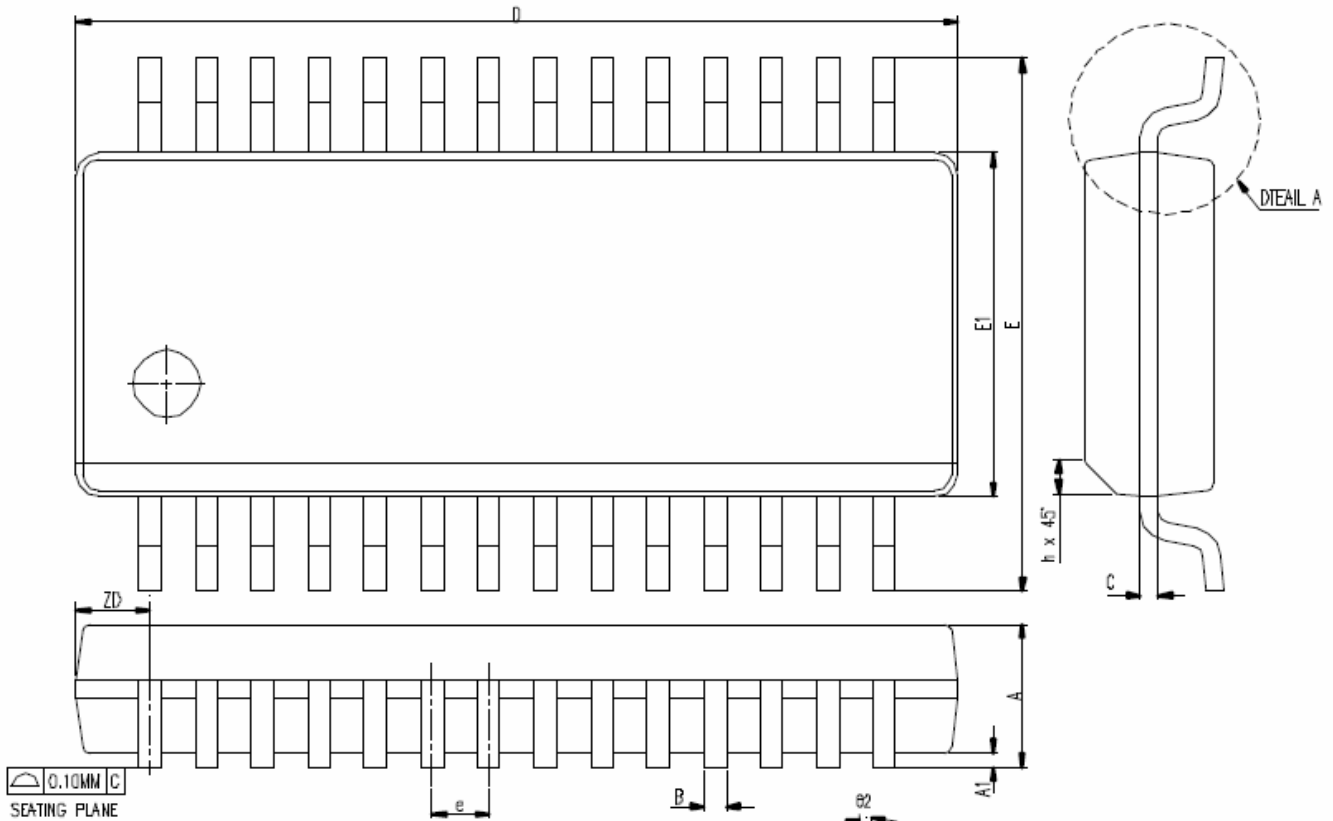




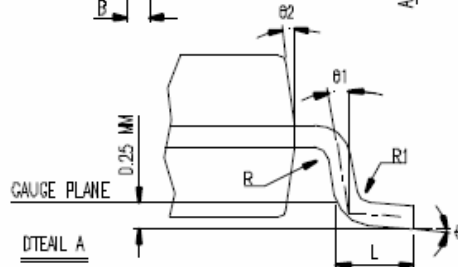
**PACKAGE OUTLINE (28 PIN SSOP)**

Package Type: SSOP-28

Package Outline Dimension



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.35	1.63	1.75	0.053	0.064	0.069
A1	0.10	0.15	0.25	0.004	0.006	0.010
A2			1.50			0.059
B	0.20		0.30	0.008		0.012
c	0.18		0.25	0.007		0.010
e	0.635 BASIC			0.025 BASIC		
D	9.80	9.91	10.01	0.386	0.390	0.394
E	5.79	5.99	6.20	0.228	0.236	0.244
E1	3.81	3.91	3.99	0.150	0.154	0.157
L	0.41	0.635	1.27	0.016	0.025	0.050
h	0.25		0.50	0.010		0.020
ZD	0.83 REF			0.033 REF.		
R1	0.20		0.33	0.008		0.013
R	0.20			0.008		
θ	0°		8°	0°		8°
θ1	0°			0°		
θ2	5°	10°	15°	5°	10°	15°
JEDEC	MO-137 (AF)					



▲ NOTES : DIMENSION D DOES NOT INCLUDE MOLD PROTRUSIONS OR GATE BURRS.  
MOLD PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.008 INCH PER SIDE.



Preliminary

**TTP229-LSF**  
**TonTouch™**

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## ORDER INFORMATION

a. Package form: TTP229-LSF

## REVISE HISTORY

1. 2010/02/25

-Original version : V\_1.0