3A, 55V H-Bridge

General Description
The LMD18200 is a 3A H-Bridge designed for motion control applications. The device is built using a multi-technology process which combines bipolar and CMOS control circuitry with DMOS power devices on the same monolithic structure. Ideal for driving DC and stepper motors; the LMD18200 accommodates peak output currents up to 6A. An innovative circuit which facilitates low-loss sensing of the output current has been implemented.

Features
- Delivers up to 3A continuous output
- Operates at supply voltages up to 55V
- Low $R_{DS(ON)}$ typically 0.33Ω per switch at 3A
- TTL and CMOS compatible inputs
- No “shoot-through” current
- Thermal warning flag output at 145°C
- Thermal shutdown (outputs off) at 170°C
- Internal clamp diodes
- Shorted load protection
- Internal charge pump with external bootstrap capability

Applications
- DC and stepper motor drives
- Position and velocity servomechanisms
- Factory automation robots
- Numerically controlled machinery
- Computer printers and plotters

 Functional Diagram

![Functional Block Diagram of LMD18200](image)
Connection Diagram and Ordering Information

11-Lead TO-220 Package
Top View
Order Number LMD18200T
See NS Package TA11B

BOOTSTRAP 2
OUTPUT 2
THERMAL FLAG OUTPUT
CURRENT SENSE OUTPUT
GROUND
V_S POWER SUPPLY
PWM INPUT
BRAKE INPUT
DIRECTION INPUT
OUTPUT 1
BOOTSTRAP 1

MOUNTING TAB CONNECTED TO GROUND (PIN 7)
## Absolute Maximum Ratings (Note 1)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

- Total Supply Voltage \( (V_S, \text{Pin 6}) \) 60V
- Voltage at Pins 3, 4, 5, 8 and 9 12V
- Voltage at Bootstrap Pins (Pins 1 and 11) \( V_{\text{OUT}} +16V \)
- Peak Output Current (200 ms) 6A
- Continuous Output Current (Note 2) 3A

### Power Dissipation (Note 3)
- Power Dissipation \( (T_A = 25°C, \text{Free Air}) \) 25W
- Storage Temperature, \( T_{\text{STG}} \) -40°C to +150°C
- Lead Temperature (Soldering, 10 sec.) 300°C

## Operating Ratings (Note 1)
- Junction Temperature, \( T_J \) -40°C to +125°C
- Supply Voltage \( V_S \) to +55V

## Electrical Characteristics (Note 5)
The following specifications apply for \( V_S = 42V \), unless otherwise specified. **Boldface** limits apply over the entire operating temperature range, \(-40°C \leq T_J \leq +125°C\), all other limits are for \( T_A = T_J = 25°C \).

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Typ</th>
<th>Limit</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{\text{DS(ON)}} )</td>
<td>Switch ON Resistance</td>
<td>Output Current = 3A (Note 6)</td>
<td>0.33</td>
<td>0.40/0.6</td>
<td>Ω (max)</td>
</tr>
<tr>
<td>( V_{\text{CLAMP}} )</td>
<td>Clamp Diode Forward Drop</td>
<td>Clamp Current = 3A (Note 6)</td>
<td>1</td>
<td>1.5</td>
<td>V (max)</td>
</tr>
<tr>
<td>( V_{\text{IL}} )</td>
<td>Logic Low Input Voltage</td>
<td>Pins 3, 4, 5</td>
<td>-0.1</td>
<td>0.8</td>
<td>V (min)</td>
</tr>
<tr>
<td>( I_{\text{IL}} )</td>
<td>Logic Low Input Current, Pins 3, 4, 5</td>
<td>( V_{\text{IN}} = -0.1V )</td>
<td>-10</td>
<td></td>
<td>μA (max)</td>
</tr>
<tr>
<td>( V_{\text{IH}} )</td>
<td>Logic High Input Voltage, Pins 3, 4, 5</td>
<td>( V_{\text{IN}} = 12V )</td>
<td>12</td>
<td></td>
<td>V (max)</td>
</tr>
<tr>
<td>( I_{\text{IH}} )</td>
<td>Logic High Input Current, Pins 3, 4, 5</td>
<td>( V_{\text{IN}} = 12V )</td>
<td>10</td>
<td></td>
<td>μA (max)</td>
</tr>
<tr>
<td>( I_{\text{OUT}} )</td>
<td>Current Sense Output, ( I_{\text{OUT}} = 1A ) (Note 8)</td>
<td></td>
<td>377</td>
<td>325/425/450</td>
<td>μA (min)</td>
</tr>
<tr>
<td>( I_{\text{OUT}} )</td>
<td>Current Sense Linearity, ( 1A \leq I_{\text{OUT}} \leq 3A ) (Note 7)</td>
<td></td>
<td>±6</td>
<td>±9</td>
<td>%</td>
</tr>
<tr>
<td>( T_{\text{JVW}} )</td>
<td>Warning Flag Temperature, Pin 9 ≤ 0.8V, ( I_L = 2 \text{ mA} )</td>
<td></td>
<td>145</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>( V_{\text{F(ON)}} )</td>
<td>Flag Output Saturation Voltage, ( T_J = T_{\text{JVW}}, I_L = 2 \text{ mA} )</td>
<td></td>
<td>0.15</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( I_{\text{F(OFF)}} )</td>
<td>Flag Output Leakage, ( V_F = 12V )</td>
<td></td>
<td>0.2</td>
<td>10</td>
<td>μA (max)</td>
</tr>
<tr>
<td>( T_{\text{JSD}} )</td>
<td>Shutdown Temperature, Outputs Turn OFF</td>
<td></td>
<td>170</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>( I_{\text{S}} )</td>
<td>Quiescent Supply Current, All Logic Inputs Low</td>
<td></td>
<td>13</td>
<td>25</td>
<td>mA (max)</td>
</tr>
<tr>
<td>( t_{\text{Don}} )</td>
<td>Output Turn-On Delay Time, Sourcing Outputs, ( I_{\text{OUT}} = 3A )</td>
<td></td>
<td>300</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{\text{Doff}} )</td>
<td>Output Turn-Off Delay Times, Sourcing Outputs, ( I_{\text{OUT}} = 3A )</td>
<td></td>
<td>200</td>
<td></td>
<td>ns</td>
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<tr>
<td>( t_{\text{on}} )</td>
<td>Output Turn-On Switching Time, Bootstrap Capacitor = 10 nF</td>
<td></td>
<td>100</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{\text{off}} )</td>
<td>Output Turn-Off Switching Time, Bootstrap Capacitor = 10 nF</td>
<td></td>
<td>75</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{\text{pw}} )</td>
<td>Minimum Input Pulse Width, Pins 3, 4 and 5</td>
<td></td>
<td>1</td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>( t_{\text{tp}} )</td>
<td>Charge Pump Rise Time, No Bootstrap Capacitor</td>
<td></td>
<td>20</td>
<td></td>
<td>μs</td>
</tr>
</tbody>
</table>
Electrical Characteristics Notes

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: See Application Information for details regarding current limiting.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is a function of $T_{J(max)}$, $\theta_{JA}$, and $T_A$. The maximum allowable power dissipation at any temperature is $P_{D(max)} = (T_{J(max)} - T_A)/\theta_{JA}$, or the number given in the Absolute Ratings, whichever is lower. The typical thermal resistance from junction to case ($\theta_{JC}$) is 1.0°C/W and from junction to ambient ($\theta_{JA}$) is 30°C/W. For guaranteed operation $T_{J(max)} = 125°C$.

Note 4: Human-body model, 100 pF discharged through a 1.5 kΩ resistor. Except Bootstrap pins (pins 1 and 11) which are protected to 1000V of ESD.

Note 5: All limits are 100% production tested at 25°C. Temperature extreme limits are guaranteed via correlation using accepted SQC (Statistical Quality Control) methods. All limits are used to calculate AOQL, (Average Outgoing Quality Level).

Note 6: Output currents are pulsed ($t_W < 2\, ms$, Duty Cycle < 5%).

Note 7: Regulation is calculated relative to the current sense output value with a 1A load.

Note 8: Selections for tighter tolerance are available. Contact factory.

Typical Performance Characteristics

![V_{SAT} vs Flag Current](image1)

![R_{DS(ON)} vs Temperature](image2)

![R_{DS(ON)} vs Supply Voltage](image3)

![Supply Current vs Supply Voltage](image4)
Supply Current vs Frequency ($V_S = 42V$)

Supply Current vs Temperature ($V_S = 42V$)

Current Sense Output vs Load Current

Current Sense Operating Region

Test Circuit

LMD18200

Test Circuit

www.national.com
### Pinout Description

(See Connection Diagram)

**Pin 1, Bootstrap 1 Input:** Bootstrap capacitor pin for half H-bridge number 1. The recommended capacitor (10 nF) is connected between pins 1 and 2.

**Pin 2, Output 1:** Half H-bridge number 1 output.

**Pin 3, Direction Input:** See Table 1. This input controls the direction of current flow between OUTPUT 1 and OUTPUT 2 (pins 2 and 10) and, therefore, the direction of rotation of a motor load.

**Pin 4, Brake Input:** See Table 1. This input is used to brake a motor by effectively shorting its terminals. When braking is desired, this input is taken to a logic high level and it is also necessary to apply logic high to PWM input, pin 5. The drivers that short the motor are determined by the logic level at the DIRECTION input (Pin 3): with Pin 3 logic high, both current sourcing output transistors are ON; with Pin 3 logic low, both current sinking output transistors are ON. All output transistors can be turned OFF by applying a logic high to Pin 4 and a logic low to PWM input Pin 5; in this case only a small bias current (approximately −1.5 mA) exists at each output pin.

**Pin 5, PWM Input:** See Table 1. How this input (and DIRECTION input, Pin 3) is used is determined by the format of the PWM Signal.

**Pin 6, V_S Power Supply**

**Pin 7, Ground Connection:** This pin is the ground return, and is internally connected to the mounting tab.

**Pin 8, Current Sense Output:** This pin provides the sourcing current sensing output signal, which is typically 377 μA/A.

**Pin 9, Thermal Flag Output:** This pin provides the thermal warning flag output signal. Pin 9 becomes active-low at 145°C (junction temperature). However the chip will not shut itself down until 170°C is reached at the junction.

**Pin 10, Output 2:** Half H-bridge number 2 output.

**Pin 11, Bootstrap 2 Input:** Bootstrap capacitor pin for half H-bridge number 2. The recommended capacitor (10 nF) is connected between pins 10 and 11.

### TABLE 1. Logic Truth Table

<table>
<thead>
<tr>
<th>PWM</th>
<th>Dir</th>
<th>Brake</th>
<th>Active Output Drivers</th>
</tr>
</thead>
<tbody>
<tr>
<td>H</td>
<td>H</td>
<td>L</td>
<td>Source 1, Sink 2</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>L</td>
<td>Sink 1, Source 2</td>
</tr>
<tr>
<td>L</td>
<td>X</td>
<td>L</td>
<td>Source 1, Source 2</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>H</td>
<td>Source 1, Source 2</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>H</td>
<td>Sink 1, Sink 2</td>
</tr>
<tr>
<td>L</td>
<td>X</td>
<td>H</td>
<td>NONE</td>
</tr>
</tbody>
</table>

### Application Information

#### Types of PWM Signals

The LMD18200 readily interfaces with different forms of PWM signals. Use of the part with two of the more popular forms of PWM is described in the following paragraphs.

**Simple, locked anti-phase PWM** consists of a single, variable duty-cycle signal in which is encoded both direction and amplitude information (see Figure 2). A 50% duty-cycle PWM signal represents zero drive, since the net value of voltage (integrated over one period) delivered to the load is zero. For the LMD18200, the PWM signal drives the direction input (pin 3) and the PWM input (pin 5) is tied to logic high.
Sign/magnitude PWM consists of separate direction (sign) and amplitude (magnitude) signals (see Figure 3). The (absolute) magnitude signal is duty-cycle modulated, and the absence of a pulse signal (a continuous logic low level) represents zero drive. Current delivered to the load is proportional to pulse width. For the LMD18200, the DIRECTION input (pin 3) is driven by the sign signal and the PWM input (pin 5) is driven by the magnitude signal.

SIGNAL TRANSITION REQUIREMENTS
To ensure proper internal logic performance, it is good practice to avoid aligning the falling and rising edges of input signals. A delay of at least 1 µsec should be incorporated between transitions of the Direction, Brake, and/or PWM input signals. A conservative approach is to be sure there is at least 500ns delay between the end of the first transition and the beginning of the second transition. See Figure 4.
**FIGURE 4. Transitions in Brake, Direction, or PWM Must Be Separated By At Least 1 μsec**

**USING THE CURRENT SENSE OUTPUT**

The CURRENT SENSE output (pin 8) has a sensitivity of 377 μA per ampere of output current. For optimal accuracy and linearity of this signal, the value of voltage generating resistor between pin 8 and ground should be chosen to limit the maximum voltage developed at pin 8 to 5V, or less. The maximum voltage compliance is 12V.

It should be noted that the recirculating currents (free wheeling currents) are ignored by the current sense circuitry. Therefore, only the currents in the upper sourcing outputs are sensed.

**USING THE THERMAL WARNING FLAG**

The THERMAL FLAG output (pin 9) is an open collector transistor. This permits a wired OR connection of thermal warning flag outputs from multiple LMD18200's, and allows the user to set the logic high level of the output signal swing to match system requirements. This output typically drives the interrupt input of a system controller. The interrupt service routine would then be designed to take appropriate steps, such as reducing load currents or initiating an orderly system shutdown. The maximum voltage compliance on the flag pin is 12V.

**SUPPLY BYPASSING**

During switching transitions the levels of fast current changes experienced may cause troublesome voltage transients across system stray inductance.

It is normally necessary to bypass the supply rail with a high quality capacitor(s) connected as close as possible to the V₅ Power Supply (Pin 6) and GROUND (Pin 7). A 1 μF high frequency ceramic capacitor is recommended. Care should be taken to limit the transients on the supply pin below the Absolute Maximum Rating of the device. When operating the chip at supply voltages above 40V a voltage suppressor (transorb) such as P6KE62A is recommended from supply to ground. Typically the ceramic capacitor can be eliminated in the presence of the voltage suppressor. Note that when driving high load currents a greater amount of supply bypass capacitance (in general at least 100 μF per Amp of load current) is required to absorb the recirculating currents of the inductive loads.

**CURRENT LIMITING**

Current limiting protection circuitry has been incorporated into the design of the LMD18200. With any power device it is important to consider the effects of the substantial surge currents through the device that may occur as a result of shorted loads. The protection circuitry monitors this increase in current (the threshold is set to approximately 10 Amps) and shuts off the power device as quickly as possible in the event of an overload condition. In a typical motor driving application the most common overload faults are caused by shorted motor windings and locked rotors. Under these conditions the inductance of the motor (as well as any series inductance in the V₅ supply line) serves to reduce the magnitude of a current surge to a safe level for the LMD18200. Once the device is shut down, the control circuitry will periodically try to turn the power device back on. This feature allows the immediate return to normal operation in the event that the fault condition has been removed. While the fault remains however, the device will cycle in and out of thermal shutdown. This can create voltage transients on the V₅ supply line and therefore proper supply bypassing techniques are required.

The most severe condition for any power device is a direct, hard-wired (“screwdriver”) long term short from an output to ground. This condition can generate a surge of current through the power device on the order of 15 Amps and require the die and package to dissipate up to 500 Watts of power for the short time required for the protection circuitry to shut off the power device. This energy can be destructive, particularly at higher operating voltages (>30V) so some precautions are in order. Proper heat sink design is essential and it is normally necessary to heat sink the V₅ supply pin (pin 6) with 1 square inch of copper on the PCB.
INTERNAL CHARGE PUMP AND USE OF BOOTSTRAP CAPACITORS

To turn on the high-side (sourcing) DMOS power devices, the gate of each device must be driven approximately 8V more positive than the supply voltage. To achieve this an internal charge pump is used to provide the gate drive voltage. As shown in Figure 5, an internal capacitor is alternately switched to ground and charged to about 14V, then switched to V supply thereby providing a gate drive voltage greater than V supply. This switching action is controlled by a continuously running internal 300 kHz oscillator. The rise time of this drive voltage is typically 20 μs which is suitable for operating frequencies up to 1 kHz.

FIGURE 5. Internal Charge Pump Circuitry

For higher switching frequencies, the LMD18200 provides for the use of external bootstrap capacitors. The bootstrap principle is in essence a second charge pump whereby a large value capacitor is used which has enough energy to quickly charge the parasitic gate input capacitance of the power device resulting in much faster rise times. The switching action is accomplished by the power switches themselves Figure 6. External 10 nF capacitors, connected from the outputs to the bootstrap pins of each high-side switch provide typically less than 100 ns rise times allowing switching frequencies up to 500 kHz.

FIGURE 6. Bootstrap Circuitry

INTERNAL PROTECTION DIODES

A major consideration when switching current through inductive loads is protection of the switching power devices from the large voltage transients that occur. Each of the four switches in the LMD18200 have a built-in protection diode to clamp transient voltages exceeding the positive supply or ground to a safe diode voltage drop across the switch. The reverse recovery characteristics of these diodes, once the transient has subsided, is important. These diodes must come out of conduction quickly and the power switches must be able to conduct the additional reverse recovery current of the diodes. The reverse recovery time of the diodes protecting the sourcing power devices is typically only 70 ns with a reverse recovery current of 1A when tested with a full 6A of forward current through the diode. For the sinking devices the recovery time is typically 100 ns with 4A of reverse current under the same conditions.

Typical Applications

FIXED OFF-TIME CONTROL

This circuit controls the current through the motor by applying an average voltage equal to zero to the motor terminals for a fixed period of time, whenever the current through the motor exceeds the commanded current. This action causes the motor current to vary slightly about an externally controlled average level. The duration of the Off-period is adjusted by the resistor and capacitor combination of the LM555. In this circuit the Sign/Magnitude mode of operation is implemented (see Types of PWM Signals).
Locked Anti-Phase Control of a brushed DC motor. Current sense output of the LMD18200 provides load sensing. The relationship of peak motor current to adjustment voltage is shown in Figure 10.

**Figure 7. Fixed Off-Time Control**

**Figure 8. Switching Waveforms**

**Torque Regulation**

LM3524D is a general purpose PWM controller. The relationship of peak motor current to adjustment voltage is shown in Figure 10.
VELOCITY REGULATION
Utilizes tachometer output from the motor to sense motor speed for a locked anti-phase control loop. The relationship of motor speed to the speed adjustment control voltage is shown in Figure 12.
FIGURE 11. Regulate Velocity with Tachometer Feedback

FIGURE 12. Motor Speed vs Control Voltage
Physical Dimensions inches (millimeters) unless otherwise noted

11-Lead TO-220 Power Package (T)
Order Number LMD18200T
NS Package Number TA11B

CONTROLLING DIMENSION IS INCH
VALUES IN 1 ARE MILLIMETERS

TA11B (Rev B)
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<thead>
<tr>
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</tr>
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<tbody>
<tr>
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<td>WEBENCH® Tools</td>
</tr>
<tr>
<td>Audio</td>
<td>App Notes</td>
</tr>
<tr>
<td>Clock and Timing</td>
<td>Reference Designs</td>
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<tr>
<td>Data Converters</td>
<td>Samples</td>
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<td>Interface</td>
<td>Eval Boards</td>
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<td>Packaging</td>
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<td>Distributors</td>
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<td>Design Made Easy</td>
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</table>

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